

NOVATECH INSTRUMENTS

INSTRUCTION MANUAL

Model 409B, 171 MHz, 4-Channel Signal Generator



Model 409B

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NOTE:

This manual applies to Model 409B with Firmware version 2.1 or later.

1.0 DESCRIPTION

1.1 The Model 409B is a four-channel Direct Digital Synthesized (DDS) Signal Generator in a small table top case with RS232 serial control. The 409B provides four independent, phase-synchronous sine wave output signals, which can be set from 0.0 Hz (DC) to 171 MHz in 0.1 Hz steps when using the internal VCTCXO clock. (Consult factory if LVCMOS signals are desired.)

1.2 The 409B can also be used with an external clock input. An on-board programmable frequency multiplier generates the system clock allowing user configured frequency ranges. The multiplier can be disabled for direct inputs up to 500 MHz for optimum phase noise performance. When used with the same external clock source, multiple 409B are phase synchronous.

1.3 A Table Mode feature enables users to store frequency, phase, amplitude and dwell time settings in static RAM. The 409B can then run through the table automatically, step through it on command from the serial port or from an external hardware trigger.

1.4 The /R option converts the External Clock input to a 10.00 MHz reference input. This option allows locking to and tracking an external 10.00 MHz reference, with no binary round-off errors. When this option is installed the accuracy and stability of the output are equal to those of the reference.

1.5 The –AC option adds two SMA connectors on the rear panel and enables synchronization of frequency, phase and amplitude updates with external devices using user provided hardware trigger signals.

1.6 The /W option provides a wireless connection between the 409B and a computer or tablet. It includes two dongles. One plugs into and is powered by the 409B and the other plugs into and is powered by the USB port on a customers computer.

2.0 SPECIFICATIONS

2.1 OUTPUTS

TYPES: Four sine simultaneously (four independent, phase-synchronous outputs).

IMPEDANCE: Sine: 50Ω; LVCMOS: 50Ω.

RANGE: 0.0 Hz to 171 MHz in 0.1 Hz steps (Sine out, int. clock).

SINE AMPLITUDE: approximately 1Vpp (+4dBm) into 50Ω. Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits), or by scale factors of 1/2, 1/4, or 1/8.

PHASE: Each channel 14-bits programmable (0.022°).

FLATNESS: ±3dB from 1 kHz to 150 MHz referenced to amplitude at 35 MHz, full scale.

2.2 LVCMOS

Voh ≥2.4V and Vol ≤0.4V when series terminated. Rise and fall times <1.5ns (>1 MHz, <125 MHz). Applies for LVCMOS Signal Outputs. Also applies for Option –AC IOUD and TS Trigger Inputs and Outputs. (Consult factory for LVCMOS Signal Outputs)

2.3 CONTROL

Output frequencies, amplitudes (10-bits) and phases (14-bits) are controlled by an RS232 serial port at 19.2kbaud. All settings (except table mode data) can be saved in non-volatile (EEPROM) memory via the RS232 port.

2.4 ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±1ppm per year, 18 to 28°C. (Internal Clock)

2.5 EXTERNAL CLOCK IN

LEVEL: 0.2 to 0.5 Vrms sine or square wave. 50Ω.

FREQUENCY: 10 MHz to 125 MHz with multiplier of 4 to 20 enabled. Direct input of 1 MHz to 500 MHz.

2.6 EXTERNAL REFERENCE (/R OPTION): External Reference must be 10.00 MHz, ±5ppm. Automatically detected. Internal clock is locked to and tracks this value.

2.7 SPECTRAL PURITY

(Typ. 50Ω load, internal clock, full-scale output)

Phase Noise: <-120dBc, 10 kHz offset, 10 MHz out.

Spurious:

<-60dBc below 10 MHz (typ. 300MHz span)

<-60dBc below 40 MHz

<-55dBc below 80 MHz

<-50dBc below 160 MHz

Harmonic:

<-65dBc below 1 MHz

<-55dBc below 20 MHz

<-45dBc below 80 MHz

<-35dBc below 160 MHz

(channel-channel isolation: <-60dBc)

2.8 TABLE MODE

On-board 4Mb static ram holds up to 32,768 profile points allowing a different output in 100μs increments.

2.9 POWER REQUIREMENTS

+4.5 to +5.5 VDC <1Amp. AC adapter provided.

2.10 SIZE

39mm H, 107mm W, 172mm L, not including connectors.

2.11 CONNECTORS

BNC for Sine Outputs and EXT CLK IN. DE9 for Serial Control. 2.5mm center positive power receptacle for +5 volts input. AC-adapter provided.

2.12 OPTIONS

OPTION /R: Changes the external clock input into a 10.00 MHz only, external input. The internal VCTCXO oscillator is phase locked to this customer supplied external 10MHz clock.

OPTION -AC: Adds IOUD and TS SMA connectors on rear panel for external control of output signal update timing. 3.3Vdc Logic pulled up via 3.3K Ohm internal resistor.

OPTION /W: Provides wireless serial communication. Uses FTDI chip set and virtual COM port.

3.0 HARDWARE INSTALLATION

3.1 Power Connection. The required power of +5Volts DC is applied through a 2.5mm center-positive power connector (Switchcraft 712A or equal). The supplied AC adapter comes with the correct mating connector.

WARNING:

Use of an unregulated source may damage the 409B. Use only the provided AC-adapter or consult Novatech Instruments for application assistance if you wish to use another power source.

3.2 Power Supply. The quality of your power supply affects the performance of the 409B. The supply should be free of ripple and noise (<50mV). Even though extensive filtering is used internal to the 409B, a quiet and well regulated power supply will ensure optimum performance. The supplied AC-adapter has been tested for proper operation.

3.3 RS232 Serial Interface Installation. The 409B is controlled by sending commands from a computer using the RS232 Serial Interface. See Table 3 for a complete set of commands. To send commands, connect your host computer to the 9-pin female RS232 connector on the rear panel of the 409B. If you are using a PC having an RS232 Serial port, a 9-pin monitor extension cable used as an RS232 cable will allow direct connection to the 409B without the use of a null modem cable or gender changer.

3.4 RS232 DE9 Connector Pinouts. The data **TO** the 409B is on pin 3; the data **FROM** the 409B is on pin 2 and the **COMMON** return is on pin 5. If Option /W is installed then 5Vdc is on pin 9.

3.5 COM Port Settings. Default 409B settings are 19.2 kBaud, 8 bits, 1 stop bit, no parity and no hardware flow control.

NOTE:

*The **SOF8_409 Software Program** is supplied on a CD with the 409B. This program provides a graphical interface, enabling simplified control of the 409B.*

3.6 USB Interface. A USB to RS232 adapter cable is available for use with computers that do not provide a serial port. Follow the manufacturer’s installation instructions when using a USB adapter.

3.7 Serial Commands. Commands are not case sensitive. There must be a space after each command except R, CLR, S and QUE commands. Commands must end with any combination of Carriage Return (CR), Line Feed (LF) or CRLF. Illegal commands will result in an error code being returned per Table 1. Table 3 on the next page lists the serial commands.

Table 1: RS232 Error Codes

Error Code	Meaning
OK	Good Command Received
?0	Unrecognized Command
?1	Bad Frequency
?2	Bad AM Command
?3	Input Line too Long
?4	Bad Phase
?5	Bad Time
?6	Bad Mode
?7	Bad Amp
?8	Bad Constant
?f	Bad Byte

3.8 Query Command. The “QUE” command returns five hexadecimal strings reflecting the present state of the 409B. See Table 2 for an explanation of the values that make up these strings.

3.9 Internal Clock. If you plan to use the 409B internal clock, which is the default setup mode, no action is required. If the 409B was previously set to use the external clock, send the serial command “C i” to reselect the internal clock. If you wish to maintain this setting, use the save command “S”.

3.10 External Clock. If you are providing your own external clock source, configure the 409B by sending the

Table 2. Response Example for QUE Command

05F5E100 0000 03FF 0000 00000000 00000000 000301
05F5E100 1000 03FF 0000 00000000 00000000 000301
05F5E100 0000 03FF 0000 00000000 00000000 000301
05F5E100 1000 03FF 0000 00000000 00000000 000301
80 BC0000 0000 6102 21
<p>Description (All values above are in hexadecimal): The lines above describe current settings for the four output channel numbers 0,1,2 and 3 in sequence. For example, Channel 0 values are: “05F5E100” = frequency in 0.1Hz steps per LSB (10MHz); “0000” = phase setting (0); “03FF” = amplitude setting(1023). The last four groups of hex values on the first four lines and the entire last line describe AD9959 and microcontroller register settings for use by the factory. The last two digits on the last line provides the 409B firmware revision number, in this case rev 2.1.</p>

serial command “C e”. Next set the system clock frequency (up to 500MHz) by sending the “Kp aa” command with your desired clock multiplier. The system clock frequency is your external clock frequency times the clock multiplier. Finally, apply your external clock to the external clock input BNC on the rear panel. Note that phase noise and stability are dependent upon your supplied clock. See specifications for signal levels required and acceptable frequency range. If you wish to maintain this setting, use the save command “S”.

CAUTION:

If the system clock frequency exceeds 500 MHz, you may overheat and damage the 409B.

Table 3: Serial Commands (Not Case Sensitive)

RS232 Command	Function
Fn xxx.xxxxxxx	Set Frequency of output “n” in MHz to nearest 0.1Hz. n=0, 1, 2, 3. Decimal point required. 0.00 sets a channel to DC. Maximum setting: 171.1276031 MHz. Single tone mode.
Pn N	Set Phase. N is an integer from 0 to 16383. Phase is set to $N*360^{\circ}/16384$ or $N*\pi/8192$ radians. Sets the relative phase of the frequency output depending upon the value of n=0, 1, 2, 3. Single tone mode.
E x	Serial echo control. x=D for Echo Disable, x=E for Echo Enable
C x	Select clock source. x=E for External clock, x=I for Internal Clock. May require adjustment of Kp and external filtering of output. (Do not use this command if the /R option is chosen.)
R	Reset. This command resets the 409B. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
A x	x=E for LVCMOS Enable, x=D for LVCMOS Disable. (Consult factory for LVCMOS.)
S	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the “CLR” command to return to default values.
QUE	Return present frequency, phase and status. Returns a character string of all internal settings.
M N	Mode command. N= 0 is puts the 409B into single tone on all channels (default). N=t puts the 409B into Table Mode for channels 0 and 1.
Vn N	Set voltage level of output. In default, the amplitude is set to the maximum: approximately 1Vpp (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1023. n=0, 1, 2, 3 to set the amplitude on frequency 0, 1, 2 or 3. If N >=1024, the scaling is turned off and the selected output is set to full scale.
Vs N	Set the output amplitude scaling factor. N=1 for full scale, N=2 for one half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
Kp aa	Set PLL reference multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01, 04 to 14). Values of Kp times clock frequency must not be between 160 MHz and 255 MHz (for internal clock, this disallows $5 \leq Kp \leq 9$).
TS	Table Step command. If the M t command is set, TS causes the 409B to step through the table. Requires all dwell settings to be “ff”. The TS command can also be executed by a negative edge on the rear mounted TS control input. (Option -AC adds the TS control input.)
Dn aaaa	Read table values. n = output channel 0 or 1. aaaa = table address.
I x	Set the I/O update pulse method. If x=a, then an I/O update is issued at the end of each serial command (default). If x=m, then a manual I/O update pulse is sent by a subsequent ‘I p’ command. If x=e then I/O update is issued when a positive 3.3V edge is applied to the rear mounted IOUD control input. (Option -AC adds the IOUD control input.)

NOTE:

When using an external clock, scaling of the “Fn” command will most likely be required. Please see Operation, Section 4, for details.

3.11 Clock Multiplier of 1. The external clock can also be used with Kp=1 for direct connection to the DDS generator. With Kp=1, the PLL multiplier is disabled. Use this direct input, up to 500 MHz, for optimum phase noise performance.

3.12 Signal Outputs. There are four signal outputs on the 409B labeled 0 to 3 on the front panel. These correspond to frequency (F0 through F3), phase (P0 through P3), and voltage (V0 to V3) commands. Simply connect your 50Ω application cable to the appropriate output BNC connector.

3.13 Rack Mounting. An optional 1U rack adapter is available for mounting up to four 409B into a rack panel. Please consult factory.

4.0 OPERATING INSTRUCTIONS

4.1 Power on reset. After power is applied, the 409B takes approximately 500ms to initialize. Commands sent during this time will be ignored or may cause erroneous operation.

4.2 Warmup. Specifications are met within approximately 15 minutes of power up.

4.3 Commands. After the 409B has been installed in the customer application system, all that is required for operation is to send the appropriate serial commands as shown in Table 3 on page 5.

4.4 Error Codes. The user host computer software must properly format the serial commands. Incorrect formatting will result in an error code being returned. See Table 1 in section 3 for a list of error codes.

4.5 Echo. For maximum interface speed, it is suggested that Echoing be disabled by using the “E d” command.

This will allow the host to send characters at a faster rate. Even when Echo is disabled, the 409B will respond with an “OK” for a correctly received data command.

4.6 Baud Rate. A special command, “Kb xx”, is available if you wish to set a baud rate that is different from the default of 19.2KBaud. The value set by this command is volatile and not saved in EEPROM. Upon power up, reset or clear, the 409B defaults to 19.2kBaud. The available “Kb xx” commands are:

- Kb 78 (Set to 9.6kBaud)
- Kb 3c (Set to 19.2KBaud)
- Kb 1e (Set to 38.4KBaud)
- Kb 14 (Set to 57.6KBaud)
- Kb 0a (Set to 115.2KBaud)

4.7 Scaling Frequency (Fn) Commands. When using the 409B default clock multiplier and the default internal master clock, the Fn command is the desired output frequency. However, if you are using an external clock you will need to send an Fn command that is different (scaled) from the desired output frequency. The calculation needed to determine this Fn command is as follows:

$$(F_{\text{command}}) = (F_{\text{out}}) (K_{\text{pi}} * F_{\text{int clk}}) / (K_{\text{pe}} * F_{\text{ext clk}})$$

Where:

F_{command} = The frequency command (Fn xxx.xxxxxxx) in MHz.

F_{out} = The desired 409B output frequency in MHz.

K_{pi} * F_{int clk} = 429.4967296 MHz. This is the default clock multiplier (15) times the default internal master clock (28.633,115,306,666,667 MHz).

K_{pe} = value of clock multiplier set by user.

F_{ext clk} = the external clock frequency in MHz.

NOTE:

Scaling is not required when option /R is installed.

4.8 Example of Frequency Scaling. For an example of scaling, suppose an external clock of 10.000 MHz is used and an output of 1.544 MHz is desired. Also assume the clock multiplier (Kp) is 15. Then:

$$(F_{\text{command}}) = (F_{\text{out}}) (K_{\text{pi}} * F_{\text{int clk}}) / (K_{\text{pe}} * F_{\text{ext clk}})$$

$$(F_{\text{command}}) = (1.544) (429.4967296) / (15 * 10)$$

$$(F_{\text{command}}) = 4.4209530$$

To set output channel 0 to 1.544 send the command “F0 4.4209539”. You should also provide an external filter or you will see excessive distortion on you output signal.

4.9 External Filters. The 409B default system clock has a nominal value of 429.4967296 MHz. When using an external clock, best performance is obtained when the actual system clock (i.e. external clock frequency times the clock multiplier setting) is close to or higher in frequency than the default, since the 409B on-board filters are optimized for the default. If the actual system clock is lower than the default, then external filtering may be needed to prevent output signal distortion. It is recommended that the external filters have roll off frequencies that are equal to or below 40% times the actual system clock frequency.

4.10 Range Bit. It is possible to control the internal range bit on the AD9959 DDS ASIC using the Kp command. For normal operation the Kp command is unmodified. However, it may be desirable that the clock multiplier gain bit be set HIGH (for external clocks where the system clock (Kp x External Clock Frequency) is from 255 to 500 MHz. To do this add hexadecimal 80 to the Kp value to be set. For the bit to be forced LOW (for external clocks where the system clock is 100 to 160 MHz), add hexadecimal 40 to the Kp value to be set.

4.11 Fractional Frequency Errors. When using the default system clock there is no fractional frequency error. However, if you use an external clock that is not identical to the internal clock then there will be a calculation round off error. The round off error as a fractional frequency error ($\Delta f/f$) for output frequencies in the MHz range will be less than 0.1ppm.

NOTE:

When using a 10 MHz external reference with Option /R installed, there is no fractional frequency error.

4.12 Phase Alignment. Phase relationships are maintained by appropriate use of the “M” and “I” commands. The “M” command has special modes “M a” and “M n”. “M a” means automatically clear phase at the end of each command. This will clear the phase register each time any command is performed. This is important when all outputs must be phase aligned. However, it will cause a phase jump in the output.

4.13 Phase Synchronous. The “M n” command turns off the automatic clearing of the phase register. This is the default mode. In this mode, the phase register is left intact when a command is performed. Use this mode if you want frequency changes to remain phase synchronous, with no phase discontinuities.

4.14 Command Execution. Further control of phase relationships and timing of command execution can be exercised by using the “I a”, “I m”, “I p” and “I e” commands. The default mode is “I a” in which a command is parsed and executed immediately following the end of the serial input sequence. In the “I m” mode, an update pulse will not be sent to the DDS chip until an “I p” command is sent. This is useful when it is important to change all the outputs to new values simultaneously. The “I e” command is used with the –AC Option.

4.15 Amplitude Matching. For applications which require precise amplitude matching between the channels, the recommended method is to use the “Vn N” command to adjust the channels to match. This command provides 10-bits of adjustment range.

4.16 Table Mode. The Model 409B contains on-board static RAM capable of storing up to 32,768 profile points. Each point contains phase, frequency, amplitude and dwell time information. The on-board microcomputer reads this RAM and programs the AD9959 DDS ASIC with the profile point data.

NOTE:

Only Channels 0 and 1 generate outputs when using the table mode.

4.17 Running a Table. An ‘m 0’ command always turns off the table mode and returns the 409B to single tone mode. If the 409B is in single tone mode, sending an “m t” command to the 409B will put it into the table mode and cause the 409B to start running the profile points stored in RAM. Sending more “m t” commands will toggle the table mode on and off.

4.18 Loading the RAM Table. The command sequence to load profile points into the RAM table is of the following form:

```
m 0
t0 0000 aabbccdd,eeff,gghh,ii
t1 0000 aabbccdd,eeff,gghh,ii
t0 0001 aabbccdd,eeff,gghh,ii
t1 0001 aabbccdd,eeff,gghh,ii
.. etc
m t
```

Where:

- m 0** puts the 409B into single tone mode.
- t0** and **t1** mean load profile points for output 0 and 1
- 0000** is a two byte hex RAM address, **t0** and **t1** must be paired with the same address.
- aabbccdd** is a four byte hex frequency setting, MSB first, 0.1 Hz resolution on LSB
- eeff** is a hex phase offset setting, MSB first, only 14-bits active
- gghh** is a hex amplitude setting, MSB first, only 10-bits active.
- ii** is dwell time, MSB first, in increments of 100µs. “00” means loop back to start, “ff” means hold present setting.
- m t** puts 409B into table mode and runs the table.

4.19 Table Formatting. Each **t0** and **t1** pair must have the same dwell setting. The “,”(comma) in each record is used as a delimiter and must be included as shown. The inputs are not case sensitive. Subsequent “m t” commands will toggle the execution of the table on and off. Upon execution of the table, the output will always begin

with address “0000” and progress until it encounters an “ff” or “00” in a dwell position. The last record in a table will be executed for 100µs if the dwell is set to “00”.

4.20 Single Stepping the Table. In single step operation all dwell times (**ii**) must be set to “ff”. Each **t0** and **t1** pair of profile points can then be stepped to the next setting by sending a TS serial command or by hardware triggering using the rear mounted TS connector (Option –AC required for hardware triggering).

4.21 Looping and Pausing the Table. If the dwell setting (**ii**) in a **t0** and **t1** profile pair are set to “00” then the table will loop back to start. If these dwell settings are set to “ff” then the table will hold the present settings.

NOTE:

The last profile pair in the table must be terminated with an “00” or “ff” in the dwell position.

4.22 Stop Running a Table. Sending an “m 0” command will stop the 409B from running the table.

4.23 Example Table for Single Stepping. This example starts with both output channels having 10MHz frequency, zero phase, and full scale amplitude then steps to 5MHz, zero phase, half scale amplitude and then repeats.

```
m 0
t0 0000 05f5e100,0000,03ff,ff
t1 0000 05f5e100,0000,03ff,ff
t0 0001 02faf080,0000,0200,ff
t1 0001 02faf080,0000,0200,ff
t0 0002 02faf080,0000,0200,00
t1 0002 02faf080,0000,0200,00
m t
ts
ts
```

“m t “ starts the table and runs the first set of “t0” and “t1” profile points.

“ts” steps to the second set of “t0” and “t1” profile points

“ts” steps to the last set of “t0” and “t1” profile points where the “00” in dwell causes the profile to run for 100 microseconds and then loop back to the start.

NOTE:

The included SOF8_409 software provides menu tools to load the table. It also uses decimal numbers instead of hex numbers. The decimal numbers are automatically converted to hex and then sent to the 409B.

4.24 Table Synchronization with External Events.

For precision timing application it is recommended that external table synchronization be used. This involves triggering table operations using customer supplied external hardware. Option -AC is required for external table synchronization. See Section 9 for detailed instructions.

4.25 Reading Table Values. The current values stored in the Table can be read by sending the “Dn aaaa” command where “n” is 0 (“t0”) or 1 (“t1”) and “aaaa” is the table address.

4.28 Table Status on Power Cycle. The RAM table is backed-up by a “supercap” for a minimum of 10 minutes. This allows for short power interrupts without losing the table information. (Consult factory for battery backup options.)

5.0 THEORY OF OPERATION

5.1 Block Diagram. Please refer to the simplified System Block Diagram in Figure 1 for the following discussion.

NOTE:

The result of the calculation of $(Kp * F_{clock})$ is referred to in this manual as the **System Clock Frequency**. The default is $Kp = 15$ and $F_{clock} = \text{internal clock} = 28.633,115,306666667 \text{ MHz}$. Thus the default system clock frequency is 429.4967296 MHz.

5.2 DDS. At every cycle of the 409B system clock, the AD9959 integrated circuit increments the phase of an internal register by a value calculated from the frequency command and sent to the AD9959 by the microcontroller. The AD9959 converts this phase value to a sinusoidal amplitude level and then sets the value of on-chip 10-bit digital-to-analog converters. The analog signals from these converters are filtered by differential 7th-order elliptical low pass filters, amplified and sent to the 409B output connectors.

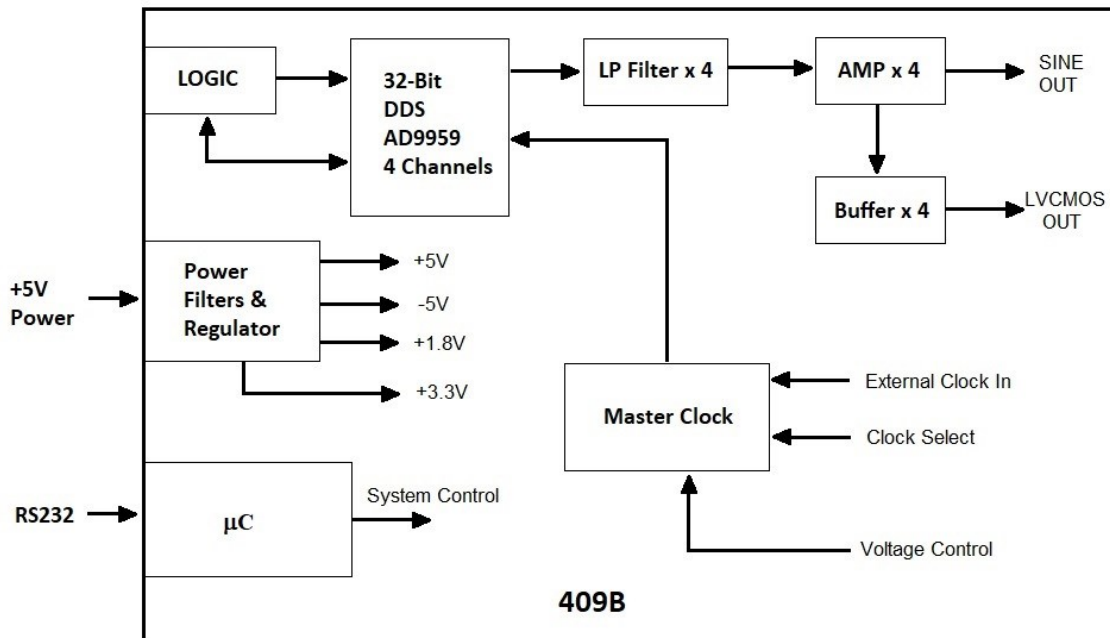


Figure 1

Simplified System Block Diagram

6.0 PERFORMANCE TEST

5.3 Clock Multiplier. The AD9959 has an internal clock multiplier of 1 or 4 to 20. This multiplier is set by the Kp command and is applied to the Master clock to produce the system clock frequency.

5.3 Frequency Calculation. The frequency generated is determined by the 32-bit frequency word sent to the 409B. The output frequency is given by:

$$F_{out} = (F_{command}) (K_p)(F_{clock}) / (2^{32})$$

Where: F_{out} = 409B output frequency in MHz.
 $F_{command}$ = Fn xxx.xxxxxxx (n=channel #)
in MHz
 K_p = AD9959 Clock Multiplier (1 or 4 to 20)
 F_{clock} = Master clock frequency in MHz. (The Master clock is either the 28.633115306666667 MHz internal clock or an external clock.)

5.4 Maximum Frequency. The 409B theoretical output frequency is limited to a maximum of 1/2 the system clock frequency. While it is possible to generate an output near 50% of the system clock, the distortion would be unacceptable. Therefore, the 409B frequency output is limited to 40% of the 429 MHz default system clock frequency by 7th-order elliptical low pass analog filters. This output limit is 171 MHz.

5.5 External Filters. External filters are NOT needed when using the 429 MHz default system clock. However, if you are using a system clock frequency substantially lower than the default, you may need an external filter with a lower cutoff frequency to obtain acceptable results. For best performance, set the corner frequency at 40% or less of your system clock frequency.

5.6 External Filter Example. When using a 10 MHz external clock, with the default clock multiplier (K_p) of 15, the system clock will be 150 MHz. An optimal external filter for this frequency would then be approximately 60 MHz (40% of 150MHz).

NOTE

External filters are NOT needed when Option /R is installed.

6.1 Setup. Install the 409B as directed in the Serial Operation part of Section 3. Connect your host controller and operate the 409B per Section 4. The test limits assume a stable environment of 18-28°C.

NOTE:

Allow the 409B to warm up for at least 15 minutes before performing any measurements. For best results, the 409B should be verified in its installed environment.

6.2 Test Equipment. See Table 4 for a list of recommended test equipment to perform the following measurements.

Table 4: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	300 MHz 50Ω	Tektronix TDS3032B
50 Termination	50Ω ±1%	Tektronix 011-0049-01 or HP53132A
Frequency Counter	180 MHz	HP53132A
Counter Time Base	10 MHz <±0.1 ppm	Novatech Instruments Model 2960AR
External Clock	400 MHz	Novatech Instruments Model 440A

6.3 Verify Frequency Accuracy. To verify the frequency of the 409B, set the output sequentially to each value in Table 5. Connect the recommended frequency counter set to 50Ω termination and 1 Hz resolution. Verify the limits show in Table 5. Test all channels to verify functionality of all outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. (LSD = Least Significant Digit on counter).

Table 5: Frequency Test Points

Frequency	Tolerance
100 kHz	$\pm 0.15 \text{ Hz } \pm 1 \text{ LSD}$
1 MHz	$\pm 1.5 \text{ Hz } \pm 1 \text{ LSD}$
10 MHz	$\pm 15 \text{ Hz } \pm 1 \text{ LSD}$
30 MHz	$\pm 45 \text{ Hz } \pm 1 \text{ LSD}$
50 MHz	$\pm 75 \text{ Hz } \pm 1 \text{ LSD}$
100 MHz	$\pm 150 \text{ Hz } \pm 1 \text{ LSD}$
170 MHz	$\pm 255 \text{ Hz } \pm 1 \text{ LSD}$

6.4 Sine Out Amplitude Verification. Set the frequency of the 409B to 10 MHz. Connect the 409B to the oscilloscope set for 50Ω termination. Set the oscilloscope to measure amplitude using at least 16 averages. Verify a reading of 1V_{pp} ±0.25V_{pp}. Repeat for the other outputs.

6.5 Amplitude Level Test. Leave the output frequency set to 10 MHz. Send the command “Vn 512” to each channel, where “n” is your channel number being tested. Verify that the amplitude on each channel decreases by one-half. Send the “R” command to reset the levels before performing the next tests.

6.6 Output Flatness Verification. Verify that the outputs are flat with frequency by performing the following test: Connect the 409B to the oscilloscope set for 50Ω termination. Use the same settings as Sine Out Amplitude Verification. Note the voltage reading.

6.7 Set the 409B to the values of Table 5. Verify that the oscilloscope amplitude reading remains within ±3dB (x1.414 to x0.707) of the value noted in the previous paragraph. (Limit upper frequency to 150 MHz.)

6.8 Repeat the output flatness verification test for each output.

6.9 External Clock Input Verification. Connect a 400 MHz external clock source via a short coaxial cable to the external clock BNC on the rear panel. Send the com-

mand “Kp 01”. Send the command “C e” to select the external clock input. Set the frequency output to 10.000 MHz by sending the command “F0 10.7374182” (scaled per section 4.0).

6.10 Verify an output of 10.0000000 MHz, ±1 Hz. You must account for any frequency errors in your external clock source.

6.11 Return the 409B to normal operation and default values by sending the “CLR” command.

6.12 This concludes the verification test of the 409B.

7.0 CALIBRATION

7.1 The 409B has two adjustable components: Y2 frequency, and R22, output amplitude. Calibration should be performed only if the 409B fails the performance test or if the unit has been repaired. Routine adjustments are not recommended nor generally required. This procedure assumes that the 409B has failed the performance test or has been repaired.

WARNING:

Calibration of the Model 409B requires that the case be opened. Calibration should be performed only by qualified personnel. The internal components are static sensitive.

7.2 Access to the adjustments is provided by removing the rear panel fasteners. Remove the two phillips head screws on the rear panel, the power receptacle nut, and the two jack-screws holding the RS232 connector. Tip the rear panel away from the instrument and slide the top cover off. Be careful not to unduly flex the connecting wires.

7.3 The adjustments shown are set to 1/2 the specification values.

NOTE:

Allow the 409B to warm up for at least 15 minutes before performing any adjustments. Do not connect any signals to the external clock connector during the adjustments. For optimum performance the 409B should be calibrated in an environment similar to its installation.

NOTE:

If your unit has the /R option installed, the oscillator adjustment is the same, except the oscillator location has moved to the adapter board.

7.4 Frequency Adjust, Y2. Set the output of the 409B to 10.0000000 MHz using the command “F0 10.0000000”. Connect output of channel 0 to your frequency counter set for 50 Ω termination. Adjust Y2 using a non-metallic adjustment tool for 10.000000 MHz, ± 7.5 Hz.

NOTE:

If the /R option is installed, access to R22 is blocked. Remove the two screws securing the /R PCB and carefully reposition the module to allow access to R22.

7.5 Amplitude Adjust, R22. Connect the output of channel 0 to the oscilloscope set to measure amplitude, with a minimum of 16 averages. Set for 50 Ω termination. Set the output to 35 MHz by sending the command “F0 35.0000000”. Adjust R22 for 1.00 Vpp ± 0.075 Vpp. This completes the calibration of the Model 409B.

8.0 OPTION /R: LOCK TO REFERENCE

8.1 The /R option consists of a small circuit board that is mounted inside the 409B. It provides locking and tracking circuitry to phase lock the internal master oscillator to an external 10 MHz reference.

8.2 The external clock input on the 409B series is changed to only accept a 10.00 MHz input. This reference input signal is automatically detected and, if within a lock range of approximately ± 5 ppm, it is locked to and tracked by a narrow-band phase lock loop.

8.3 If an input signal is not detected, the unit will default to the internal free-running oscillator and perform identically to a 409B without the /R option.

8.4 The front panel LED will display four conditions:

Steady Green: unit is locked to a stable external reference or is using the internal free running master clock.

Blinking Green: unit is stabilizing to a free running condition. This occurs upon powerup or if the reference is removed.

Steady Red: unit detects an external input, but cannot lock to it.

Blinking Red: unit has detected a 10MHz external signal and is attempting to lock. This will occur if the 409B had previously been free running.

8.5 When changing the reference mode, the phase lock loop may take several minutes to stabilize to the final resolution of the 409B. Changing from a blinking LED to a stable LED indicates that the process is completing, but you should verify the outputs.

8.6 The /R option disables the “C E” command functionality so that it is no longer valid and should not be used. The clock multiplier default value of 15 should not be changed and the “Kp” command should not be used. If either the “C E” or “Kp” command is used with the /R option, you will get unpredictable behavior.

9.0 OPTION –AC: EXTERNAL TIMING CONTROL.

9.1 Description. Option –AC adds two rear mounted SMA connectors, labeled IOUD and TS, that can be used for triggering and synchronizing 409B outputs.

9.2 IOUD Output vs Input. By default, the signal on the IOUD connector is an output indicating that the microcontroller has triggered an update to the 409B front panel sine wave outputs. Sending the “I e” command changes the IOUD from an output to an input and requires that an external trigger pulse be applied to the IOUD connector to update the 409B outputs.

9.3 IOUD Used as Output. The IOUD signal is pulled up internally to 3.3Vdc through a 3.3K Ohm resistor. When the 409B microcontroller updates the 409B, it pulses IOUD low for about 250 nanoseconds. The actual trigger happens on the rising edge of this signal and this rising edge can be read by the users hardware.

9.4 TS Input. The TS connector is always an input. It functions just like the “ts” serial command. If a table is running and is configured for single stepping, then applying a trigger signal to the TS connector will step through the table. The TS input is pulled up to 3.3Vdc inside the 409B by a 3.3K Ohm resistor. To trigger the TS input, the user should pull it to ground. The negative edge will then trigger the input. An edge occurring sooner than 100µs from the previous TS trigger will be ignored. Detection of the edge is affected by the current state of the microcontroller processing.

9.5 Microcontroller Triggering of the Table. This is the default process and the IOUD connector must be in the default output configuration. In response to an “m t” or “ts” serial command or to a TS connector trigger input, new settings are moved from table RAM into registers in the AD9959 DDS ASIC. This takes about 100µs. The microcontroller then puts a 250 nanosecond trigger pulse on the IOUD pin. The rising edge of this trigger causes the AD9959 DDS ASIC to update both table output channels within 100 ±8 nanoseconds.

9.4 Configuring IOUD as an Input. Sending an “I e” command will change the IOUD connector from an output to an input. This 3.3Vdc logic input is held high with a 3.3K ohm pullup resistor. Triggering the 409B to update the front panel outputs will then require an external hardware trigger be applied to the IOUD connector. Sending an “s” command will store the current state of the “I e” register.

9.5 External Triggering when IOUD is an Input. The AD9959 DDS ASIC must be preloaded with a new set of values about 100µs prior to applying an IOUD trigger. Preloading is done with the “m t” or “ts” command or by applying a trigger signal to the TS connector. Once preloaded, the 409B can be triggered to update all outputs by applying a trigger pulse to the IOUD connector. The trigger signal must pull IOUD low for a minimum of 10 nanoseconds and then pulse it high (can remain high) for a minimum of 10 nanoseconds. The trigger will happen on the rising edge. The update to the outputs will have a pipeline delay of less than 100 nanoseconds ± 8 nanoseconds from the positive edge of the IOUD trigger signal.

9.6 More Precise Timing with External Triggering. Using external triggering enables the user to take control of exactly when the outputs are updated. This avoids the uncertainty regarding the exact amount of time the processor will take to move data from RAM to the AD9959 DDS ASIC registers. While the user must still allow 100 µs of time for this data to move, the timing of the trigger update is decoupled from this time uncertainty. This method also enables the user to more easily synchronize updates with external events. External triggering can be used with the table mode and it can also be used when the table mode is off and the user is sending serial commands.

9.7 409B Initialization Issue. Please note that the 409B needs to take control of the IOUD pin during 409B initialization. Initialization happens when power is applied to the 409B or after a reset command has been sent. For this reason, the user should not connect external signals to the IOUD connector during an initialization process.

10.0 OPTION /W WIRELESS SERIAL INTERFACE



10.1 Description. The /W option provides plug and play wireless communication between the Model 409B and a computer or tablet. There is no user setup or software required to use option /W. The dongles are a matched set so both dongles must have the same serial number.

10.2 Hardware. Option /W includes a dongle with a DB9 connector that plugs into the rear of the Model 409B and communicates wirelessly with a second dongle that has a USB connector.

NOTE:

The plastic cap on the USB dongle should be removed and installed by applying pressure on one corner of the cap. Do not try to pull it straight off.

10.3 Power. The DB9 dongle is powered by 5Vdc from the 409B. This 5Vdc is present on pin 9 of the 409B serial connector on 409B units that have the /W box marked on the rear panel. The USB dongle is powered by the customer's computer or tablet.

10.4 Range. The wireless communication range is approximately 30 feet. A solid green light on the DB9 dongle indicates that the two dongles are communicating wirelessly.

10.5 USB Dongle Virtual COM Port. The USB dongle uses the FTDI chipset. Most computers will automatically download the FTDI driver and set up a virtual COM port when the USB dongle is plugged into the computer. If this is not done automatically, then the user may have to download the driver from the FTDI website manually. The FTDI driver download page is located at “<https://www.ftdichip.com/drivers/VCP.htm>“ The USB dongle has been tested successfully with Android devices running the “Serial USB Terminal” Android application that is available from Google Play.

NOTE:

You can control multiple 409B from one computer by using multiple Option /W USB dongles or multiple USB to Serial Adapters. Your computer will assign a different COM port number to each USB device. You can also run multiple copies of the SOF8_409 software and set them to different COM port numbers.

10.6 Installing Option /W. Install the USB dongle into a USB 2.0 or later port on a computer. Note the flashing blue light indicating it is receiving power. With the power to the 409B disconnected, plug the DB9 dongle into the 9-pin serial connector on the rear of the 409B. Verify that both dongles have the same serial number. Apply power to the 409B and observe that the DB9 dongle flashes green for about five seconds and then turns solid green and the blue light on the USB dongle turns solid blue. The solid lights indicate that Option /W is successfully communicating.

10.7 COM Port Settings. Once Option /W is installed you can use the SOF8_409 “COM Port/View Available COM Port” menu to assist in identifying the virtual COM port number that the computer has assigned to the USB dongle. You can also use the windows device manager to find this COM port number. The virtual COM port must be configured for 19.2kBaud, 8 bits, 1 stop bit, no parity, no hardware flow control. If you are using the SOF8_409 program it will automatically configure the selected COM port to these settings.

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WARRANTY

NOVATECH INSTRUMENTS warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS.

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