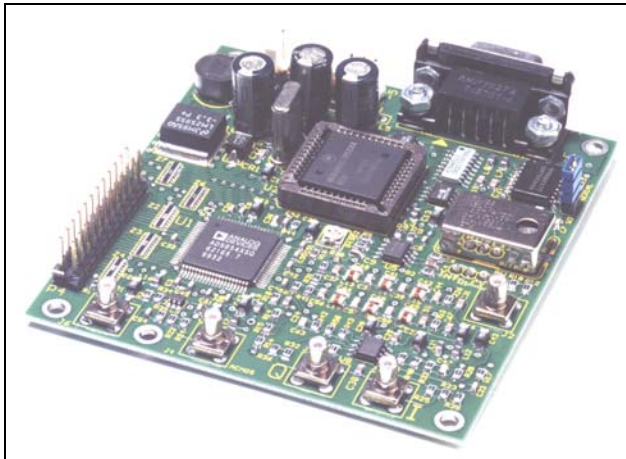


# NOVATECH INSTRUMENTS

## 100MHz Quadrature Signal Generator Module Model DDS8m



The DDS8m is a 100MHz Direct Digital Synthesized Signal Generator on a small circuit board. The DDS8m generates Sine/Cosine and AC/MOS/TTL output signals simultaneously up to 100MHz in 1 $\mu$ Hz steps under RS232 or binary parallel control. Sweep, FSK, Chirp, and Single Tone are generated on board. The parallel binary interface allows control up to 100MHz of all parameters. The RS232 interface uses simple commands to control the module and allows non-volatile storage of all settings. The DDS8m is equipped with a  $\pm 1.5$ ppm on-board TCXO clock or it can accept an external clock source up to 300MHz.

### Specifications:

#### OUTPUTS

TYPES: Sine, Cosine and AC/MOS/TTL simultaneously.  
IMPEDANCE: 50 $\Omega$

RANGE: 100Hz to 100MHz in 1 $\mu$ Hz steps (int. clock).

SINE/COS AMPLITUDE: approximately +7dBm (0.5Vrms) into 50 $\Omega$  load. Programmable from 0/4096 to 4095/4096 of Full Scale (12 bits internal control).

FLATNESS:  $\pm 3$ dB from 10kHz to 100MHz referenced to amplitude at 30MHz, stable to  $< \pm 1$ dB from 18-28 $^{\circ}$ C.

CLOCK OUTPUT: Approximately 1Vpp level clock at the oscillator or external clock frequency. 50 $\Omega$ .

#### AC/MOS/TTL AMPLITUDE

$V_{OL} < 0.5V$ ,  $V_{OH} > 2.5V$  into a series terminated 15pF load.

$T_{r,f} < 5ns$ . Duty Factor: 45-55%. 50 $\Omega$ .

#### CONTROL

Output frequencies, phase (14 bits) and modes are controlled either by an RS232 serial port at 19.2kbaud or a byte-parallel port. RS232 control allows nonvolatile storage of settings. Control method is jumper selectable and detected upon power up. (see Model DDS8p for a fast parallel binary version).

#### ACCURACY AND STABILITY

Accuracy:  $< \pm 1.5$ ppm at 10-40 $^{\circ}$ C. Stable to an additional  $\pm 1$ ppm per year, 18-28 $^{\circ}$ C. (Internal Clock)

#### EXTERNAL CLOCK IN

LEVEL: 0.35-2.5Vrms Sine or Square Wave. 50 $\Omega$ .

FREQUENCY: 5MHz to 75MHz. Multiplier of 4x to 20x

selected via control port (may be bypassed for up to 300MHz direct input). (Output may require additional filtering for optimum performance with external clock.)

#### SPECTRAL PURITY (Typ. 50 $\Omega$ load, internal clock)

Phase Noise:  $< -140$ dBc, 10kHz offset, 5MHz out.

Spurious:  $< -70$ dBc below 10MHz (typ. 200MHz span)

Harmonic:  $< -65$ dBc below 40MHz  
 $< -50$ dBc below 100MHz  
 $< -65$ dBc below 1MHz  
 $< -60$ dBc below 10MHz  
 $< -50$ dBc below 20MHz  
 $< -40$ dBc below 50MHz  
 $< -35$ dBc below 100MHz

#### SWITCHING TIME

Parallel Control: Output changes at up to 15MHz depending upon customer supplied hardware. RS232 control depends upon host speed and commands sent, typ.  $< 10ms$  for a new frequency. (DDS8p: 600ns)

#### POWER REQUIREMENTS

4.75 to 5.25V@  $< 1.0A$  and -5.25 to -4.75V@  $< 100mA$ .

#### SIZE

82.6mm by 88.9mm circuit board. Max. height 17mm.

#### CONNECTORS

SMB for Cosine(I)/Sine(Q), AC/MOS/TTL, CLK OUT and EXT CLK IN. 3-pin header for Power. 24-pin header for parallel control.

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**Table 2: RS232 Serial Commands**

| <b>RS232 Command</b> | <b>Function</b>  |
|----------------------|--|
| F0 XX.XXXXXXXXXXXXXX | Set Frequency in MHz to nearest 1μHz. Decimal point required.  |
| F1 XX.XXXXXXXXXXXXXX | Start Frequency in MHz to nearest 1μHz. Decimal point required. Same as F0 if Mode 0 is selected.  |
| F2 XX.XXXXXXXXXXXXXX | Stop Frequency in MHz to nearest 1μHz. Decimal point required. Modes 1 and 2.  |
| Fd XX.XXXXXXXXXXXXXX | Delta Frequency in MHz. Software sets to nearest 1μHz. Decimal point required.   |
| E x                  | x=D for Echo <b>Disable</b> , x=E for Echo <b>Enable</b>   |
| Q x                  | x=D for Q-channel <b>Disable</b> , x=E for Q-channel <b>Enable</b>   |
| R                    | Reset. This command resets the DDS8m. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.   |
| CLR                  | Clear. This command clears the EEPROM valid flag and restores all factory default values.  |
| Px N                 | Set Phase. N is an integer from 0 to 16383. Phase is set to $N*360^{\circ}/16384$ or $N*\pi/8192$ radians. Sets either the phase P1 or P2 depending upon the value of x (1 or 2). The I and Q outputs are always nominally 90°. In Mode 0, this sets the static phase. In Mode 4, the phase is either P1 or P2 depending upon the state of Pin 8 of the parallel connector.  |
| A x                  | x=E for AC MOS/TTL <b>Enable</b> , x=D for AC MOS/TTL <b>Disable</b>   |
| S                    | Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the "CLR" command to return to default values.   |
| QUE                  | Return present frequency, phase and status. Returns an 80-character string of all internal settings: hexadecimal format. See Table 7.  |
| M N                  | Mode command. N is 0, 1, 2, 3 or 4. 0 is Single Tone, 1 is FSK (pin 8 of parallel port is active), 2 is Triangular Ramped Frequency, 3 is Chirp Frequency and 4 is BPSK (pin 8 is active). Defaults to Mode 0 upon turn-on, unless another mode is saved. See Appendix A.  |
| Td N                 | Time at each Fd (see Appendix A). N is an integer from 0 to a maximum value of $2^{20}-1$ or 1048575. Applies to modes 2 and 3 only. Approximately 3.5ns increments using internal clock. In mode 2, frequency ramps from F1 to F2 and returns to F1 continuously in steps of Fd at time intervals of Td.  |
| Tr N                 | Repeat time in mode 2 and 3. In mode 3, the frequency will ramp starting at F1 in steps of Fd, at time intervals Td, until Tr times out, repeating continuously from F1. N is an integer between 5 and $2^{32}-1$ (4294967295). Approximately 7.0ns increments with the internal clock. A 3.3V CMOS level pulse at the start of each ramp is provided on Pin 10 of the parallel I/O connector. Approximately 40ns (8 system clocks) wide for the internal clock. In Mode 2, Tr sets the timing of an external trigger pulse on Pin 10 of the parallel interface. |
| Vx N                 | Set voltage level of output. In default, the amplitude is set to the maximum: approximately +7dBm into 50Ω. N can range from 0 (off) to 4095 (no decimal point allowed). Voltage level is scaled to $N/4096$ . x is I or Q to set the amplitude on the I or Q channel. If $N > 4095$ , the scaling is turned off and both outputs are set to maximum. Overrides the "Z" command.   |
| Kp aa                | Set PLL reference multiplier constant. Must be one Hex byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 ( $01_h$ , $04_h$ to $14_h$ ).  |
| Z N                  | Turns on 30% Amplitude Modulation of Cosine (I) channel output. N is the frequency of modulation in 100Hz steps, 900Hz maximum (9). $N = 0$ turns off modulation. Use of this command overrides the V command on the I channel. Entering any "M" command turns off modulation.   |
| <b>B aadd</b>        | Set a data byte "dd" at address "aa" in Hex. Allows setting of all internal registers. "aa" is in the range of $00_h$ to $27_h$ while "dd" is from $00_h$ to $ff_h$ . No error checking, other than correct format, is performed. It is possible to set the DDS8m into a nonfunctional state requiring a power cycle to recover with this command. Some internal modes may require excessive power and may permanently damage the DDS8m (for debugging).   |