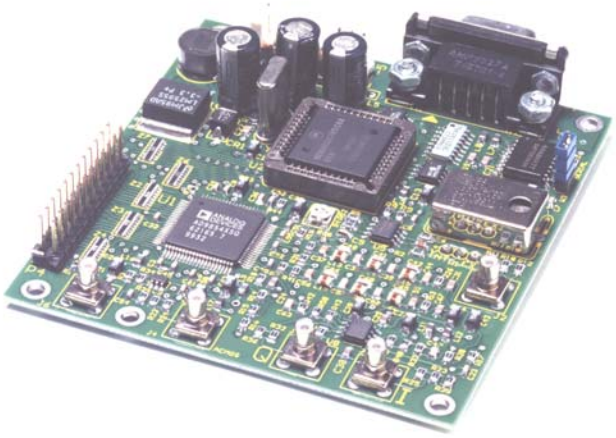
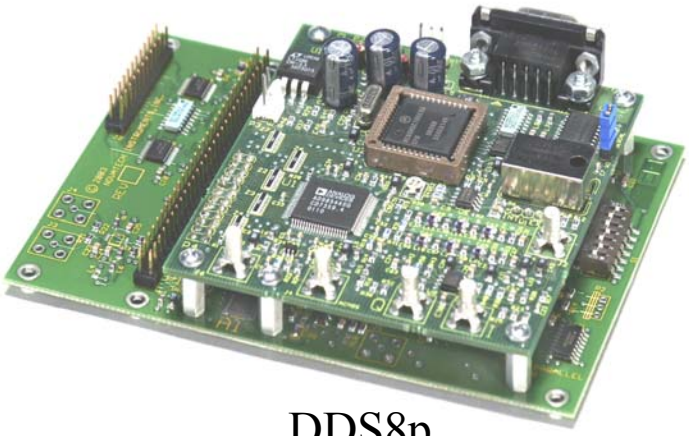
NOVATECH
INSTRUMENTS

INSTRUCTION MANUAL
Model DDS8m&p 100MHz&120MHz Quadrature Signal Generator Modules



DDS8m



DDS8p

DDS8m&p
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1.0 DESCRIPTION

1.1 The Model DDS8m is a 100MHz Quadrature **D**irect **D**igital **S**ynthesizer (DDS) on a small printed wiring module with both byte-parallel and RS232 serial control. The DDS8m provides both Cosine(I), Sine(Q) and 3.3V ACMOS output signals, which can be set from 100Hz to 100MHz in 1μHz steps when using the internal VCTCXO (voltage controlled temperature compensated crystal oscillator) clock (120MHz for the DDS8p).

1.2 The DDS8m can also be used with an External Clock input. An on-board programmable frequency multiplier generates the master clock allowing user configured frequency ranges. The multiplier can be disabled for direct inputs up to 300MHz for optimum phase noise performance. When used with an external clock, multiple DDS8m are phase synchronous. The Clock Out from one DDS8m may be used as an external clock source for daisy chaining additional DDS8m.

1.3 The DDS8p is similar to the DDS8m, but a fast parallel binary bus has been added to control phase and frequency. The DDS8p allows frequency and phase agile control of the DDS8m. **See Appendix B for details on the DDS8p parallel board.**

2.0 SPECIFICATIONS (DDS8m)

2.1 OUTPUTS

TYPES: Sine, Cosine and ACMOS/TTL Simultaneously.
IMPEDANCE: 50Ω.
FREQUENCY: 100Hz to 100MHz in 1μHz steps, using Internal Clock. ($1x10^{-13}$ resolution @10MHz)
CLOCK OUTPUT: Approximately 1Vpp level clock at the oscillator or external clock frequency. 50Ω: will drive additional DDS8m when applied to their external clock input. Useful to 50MHz.

2.2 SINE/COSINE AMPLITUDE

AMPLITUDE: Approximately 0.5Vrms (+7dBm) into 50Ω. Programmable from 0/4096 to 4095/4096 of Full Scale (12 Bits).
FLATNESS: ±3dB from 100kHz to 100MHz referenced to amplitude at 30MHz, stable to ±1dB from 18-28 ºC.

2.3 ACMOS/TTL AMPLITUDE

V_{OL}<0.5V, V_{OH}>2.5V into a 15pF load, series terminated. Rise and Fall Times <5ns. Duty Factor: 45-55%. 50Ω output impedance. Use series or capacitively-coupled parallel termination.

2.4 ACCURACY AND STABILITY

Accurate to <±1.5ppm at 10-40ºC. Stable to an additional ±1ppm per year, 18-28ºC. External voltage of 0 to 5 volts will adjust the on-board VCTCXO ±5ppm.

2.5 EXTERNAL CLOCK INPUT

LEVEL: 0.35-2.5Vrms Sine or Square Wave can be applied to the EXT CLK Input SMB. 50Ω.
FREQUENCY: Input range of 5MHz to 75MHz. Programmable frequency multiplier (4x to 20x) on board. Multiplier can be bypassed for direct input to 300MHz. An external filter may be required for optimum performance.

2.6 **SPECTRAL PURITY** (Typ. 50Ω load, int clk)
Phase Noise: <-140dBc, 10kHz offset, 5MHz out.
Spurious: <-70dBc below 10MHz (200MHz span)
<-65dBc below 40MHz
<-60dBc below 60MHz
<-50dBc below 100MHz
Harmonic: <-70dBc below 1MHz
<-60dBc below 10MHz
<-50dBc below 20MHz
<-40dBc below 50MHz
<-35dBc below 100MHz

2.7 CONTROL (DDS8m)

Output Frequency and phase (14-bits) are controlled either by an RS232 serial port at 19.2kBaud or a byte-parallel binary port. RS232 control allows non-volatile storage of settings. The control method is jumper selectable and detected upon power up. Parallel port signals are 3.3v VHCMOS logic compatible.

2.8 SWITCHING TIME

Byte Parallel Control: Output changes in approximately 0.6μs, depending upon customer supplied

hardware. RS232 control depends upon host speed and commands sent, typically <10ms for a new frequency. See Model DDS8p (Appendix B) for the high-speed binary parallel interface version of the DDS8m.

2.9 POWER REQUIREMENTS
+4.75 to +5.25V @<0.75A; -5.25 to -4.75V @<100mA.

2.10 SIZE
82.6mm by 88.9mm card. Max. height: 17mm.

2.11 CONNECTORS
SMB for SINE(Q), COSINE(I), ACMOS/TTL, CLK OUT and EXT CLK IN. 3-pin Header for power. 24-pin for Parallel Control. 2-pin Header for Voltage Control.

3.0 HARDWARE INSTALLATION

WARNING:

The DDS8m contains static sensitive components. Before opening the package, follow appropriate static precautions. Failure to follow static precautions may damage the DDS8m.

3.1 **Power Connection.** Figure 1, Connection Placement Diagram, shows a top view of the DDS8m module. The required power of ±5 Volts DC is applied through a 3-pin connector (mates with Amp 640621-3). If you are using a Novatech Instruments, Inc. supplied connector, Red is +5, Blue is -5 and Black is the common return.

3.2 The quality of your power supply may affect the performance of the DDS8m. The supply should be free of ripple and noise (<50mV). Even though extensive filtering is used on the DDS8m board, a quiet and well regulated power supply will ensure optimum performance. If switching power supplies are used, please verify that your system noise requirement is met.

NOTE:

The DDS8m generates its internal +3.3V from your supplied +5V. If your system has +3.3V available, consult Novatech Instruments, Inc. regarding a DDS8m with a separate +3.3V input. This will reduce total system power requirements.

3.3 **RS232 Installation.** To use the DDS8m in the RS232 mode, verify that jumper W3 is installed before power-up and connect your host computer to the 9-pin female RS232 connector on the DDS8m. If you are using a PC, a 9-pin monitor extension cable used as an RS232 cable will allow direct connection to the DDS8m without the use of a null modem cable or gender changer. If you are using a different computer, terminal or other control source, please note that the data **TO** the DDS8m is on pin 3; the data **FROM** the DDS8m is on pin 2 and the **COMMON** return is on pin 5. Set your host to 19.2 kbaud, 8 bits, 1 stop bit, no parity and no hardware flow control. See Table 2 for RS232 Serial Commands.

3.4 Commands are not case sensitive. There must be a space after each command except `R`, `CLR`, `S` and `QUE`. End with any combination of `CR`, `LF` or `CRLF`. Illegal commands will result in an error code being returned per Table 1.

Table 1: RS232 Error Codes

Error Code	Meaning
`OK`	Good command received (not sent for R, CLR and QUE)
`?0`	Unrecognized Command
`?1`	Bad Frequency
`?2`	Bad AM Command
`?3`	Input line too long
`?4`	Bad Phase
`?5`	Bad Time
`?6`	Bad Mode
`?7`	Bad Amp
`?8`	Bad Constant
`?f`	Bad Byte

3.5 The "`QUE`" command returns a string of 80 Hexadecimal (Hex) characters. The characters represent the present state of all the registers internal to the DDS8m. See Table 7 for the addresses that make up this string. Note that the frequency will be scaled as discussed below if an external clock is used.

3.6 The command in "***`Bold Italic`***" (***"B"***) can cause erroneous operation and must be used with

Table 2: RS232 Serial Commands

RS232 Command	Function
F0 XX.XXXXXXXXXXX	Set Frequency in MHz to nearest 1μHz. Decimal point required.
F1 XX.XXXXXXXXXXX	Start Frequency in MHz to nearest 1μHz. Decimal point required. Same as F0 if Mode 0 is selected.
F2 XX.XXXXXXXXXXX	Stop Frequency in MHz to nearest 1μHz. Decimal point required. Modes 1 and 2.
Fd XX.XXXXXXXXXXX	Delta Frequency in MHz. Software sets to nearest 1μHz. Decimal point required.
E x	x=D for Echo **D**isable, x=E for Echo **E**nable
Q x	x=D for Q-channel **D**isable, x=E for Q-channel **E**nable
R	Reset. This command resets the DDS8m. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
Px N	Set Phase. N is an integer from 0 to 16383. Phase is set to N*360^o/16384 or N*π/8192 radians. Sets either the phase P1 or P2 depending upon the value of x (1 or 2). The I and Q outputs are always nominally 90^o. In Mode 0, this sets the static phase. In Mode 4, the phase is either P1or P2 depending upon the state of Pin 8 of the parallel connector.
A x	x=E for ACMOS/TTL **E**nable, x=D for ACMOS/TTL **D**isable
S	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the "CLR" command to return to default values.
QUE	Return present frequency, phase and status. Returns an 80-character string of all internal settings: hexadecimal format. See Table 7.
M N	Mode command. N is 0, 1, 2, 3 or 4. 0 is Single Tone, 1 is FSK (pin 8 of parallel port is active), 2 is Triangular Ramped Frequency, 3 is Chirp Frequency and 4 is BPSK (pin 8 is active). Defaults to Mode 0 upon turn-on, unless another mode is saved. See Appendix A.
Td N	Time at each Fd (see Appendix A). N is an integer from 0 to a maximum value of 2^{20}-1 or 1048575. Applies to modes 2 and 3 only. Approximately 3.5ns increments using internal clock. In mode 2, frequency ramps from F1 to F2 and returns to F1 continuously in steps of Fd at time intervals of Td.
Tr N	Repeat time in mode 2 and 3. In mode 3, the frequency will ramp starting at F1 in steps of Fd, at time intervals Td, until Tr times out, repeating continuously from F1. N is an integer between 5 and 2^{32}-1 (4294967295). Approximately 7.0ns increments with the internal clock. A 3.3V CMOS level pulse at the start of each ramp is provided on Pin 10 of the parallel I/O connector. Approximately 40ns (8 system clocks) wide for the internal clock. In Mode 2, Tr sets the timing of an external trigger pulse on Pin 10 of the parallel interface.
Vx N	Set voltage level of output. In default, the amplitude is set to the maximum: approximately +7dBm into 50Ω. N can range from 0 (off) to 4095 (no decimal point allowed). Voltage level is scaled to N/4096. x is I or Q to set the amplitude on the I or Q channel. If N >4095, the scaling is turned off and both outputs are set to maximum. Overrides the "Z" command.
Kp aa	Set PLL reference multiplier constant. Must be one Hex byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01_h, 04_h to 14_h).
Z N	Turns on 30% Amplitude Modulation of Cosine (I) channel output. N is the frequency of modulation in 100Hz steps, 900Hz maximum (9). N = 0 turns off modulation. Use of this command overrides the V command on the I channel. Entering any "M" command turns off modulation.
B aadd	Set a data byte "dd" at address "aa" in Hex. Allows setting of all internal registers. "aa" is in the range of 00_h to 27_h while "dd" is from 00_h to ff_h. No error checking, other then correct format, is performed. It is possible to set the DDS8m into a nonfunctional state requiring a power cycle to recover with this command. Some internal modes may require excessive power and may permanently damage the DDS8m (for debugging).

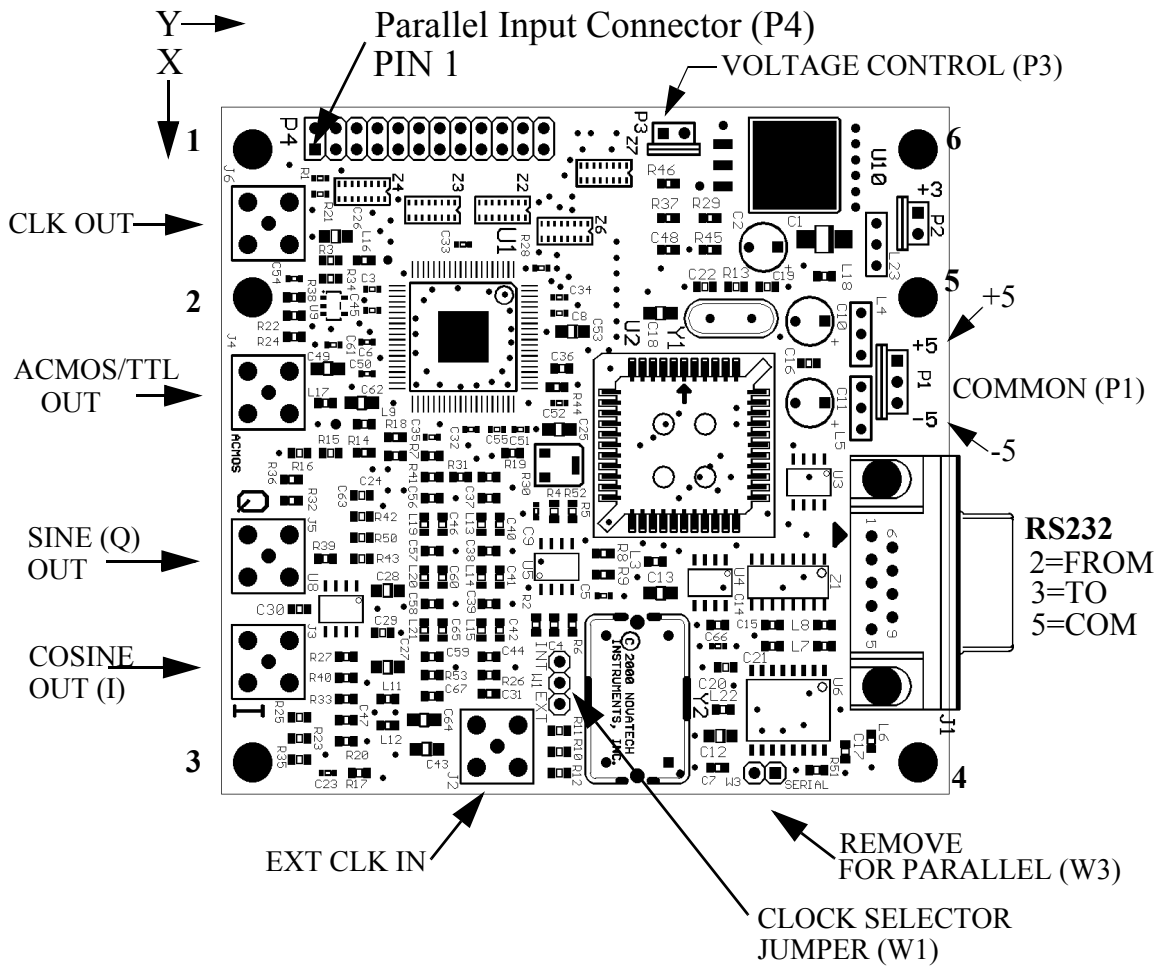


Figure 1: DDS8m Placement Diagram (no scale)

Table 3: Mounting Hole Locations (hole size: 3.15mm), DDS8m

Hole Number	Location (x,y) mm
1	5.08, 3.81
2	22.86, 3.81
3	78.74, 3.81
4	78.73, 85.09
5	22.86, 85.09
6	5.08, 85.09

Pin Number	Function	Type	Pin Number	Function	Type
1	Ground (Power Supply Common)	PS	2	+3.3V (Power Supply Reference, 50mA max)	PS
3	Ground (Power Supply Common)	PS	4	MR (Master DDS Reset)	I
5	IRQ- (must be left unconnected unless used for special modes, see appendix)	--	6	KEYING	I
7	RDB- (ReaD Byte)	I	8	FSK	I
9	WRB- (WRite Byte)	I	10	IOUD	I/O
11	A0 (Address, LSB)	I	12	A1	I
13	A2	I	14	A3	I
15	A4	I	16	A5 (MSB)	I
17	D0 (Data, LSB)	I/O	18	D1	I/O
19	D2	I/O	20	D3	I/O
21	D4	I/O	22	D5	I/O
23	D6	I/O	24	D7 (MSB)	I/O

Table 4: Byte Parallel Connector Pinout (DDS8m only)

WARNING:

All these signals are 3.3Volt CMOS. You must provide level shifting or buffering if connection to a 5Volt logic system is being made. VHC buffers are suggested. Otherwise permanent damage may result.

Table 5: DDS8m Serial Firmware Modes

Operating Mode	Parameters Required
0, Single Tone	F0
1, FSK	F1, F2, connection to Pin 8
2, Ramped FSK	F1, F2, Fd, Td, Tr
3, Chirp	F1, Fd, Td, Tr, connection to Pin 8
4, BPSK	F0 or F1, P1, P2, connection to Pin 8

Figure 2: Byte Parallel Input Timing Diagram (DDS8m)

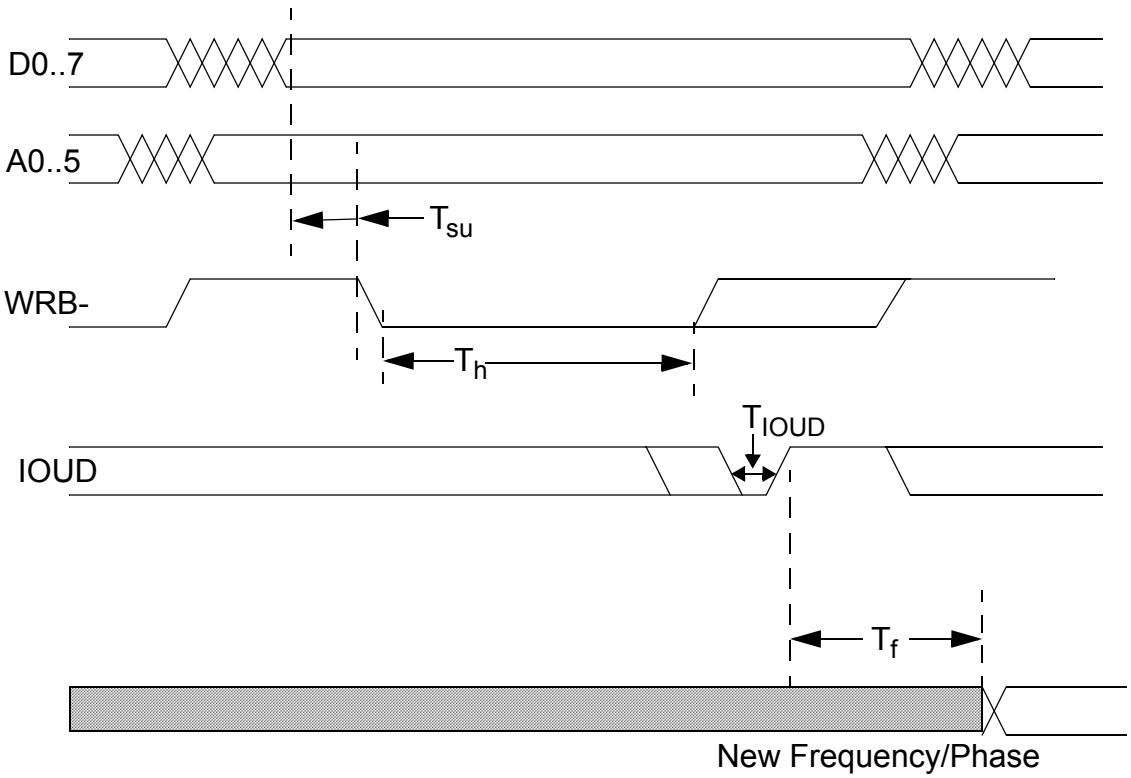


Table 6: DDS8m Byte Parallel Control Timing

Parameter	Name	Min	Max	Notes
T_{su}	Data Setup Time	10ns	--	
T_h	Write Hold Time	15ns	--	Address and Data must remain stable during this time.
T_f	New Frequency Update Time		170ns	value shown for internal clock (approximately 45 master clock cycles)
T_{IOUD}	I/O Update Time	15ns	--	Minimum high/low time. Data latches and transfers to working registers on positive edge.

care. Contact Novatech Instruments, Inc. for application assistance if you feel you need to use this command, which is intended for "debugging" purposes.

3.7 **Byte Parallel Installation.** The DDS8m can also be controlled by a byte-parallel binary connection made to the 24-pin (12x2) header. See Table 4 for connector pinout and pin descriptions. For byte-parallel operation, W3 must be removed before power is applied. (See Appendix B for the DDS8p binary parallel version.)

NOTE:

*The windows program **SOF8** is available from Novatech Instruments, Inc. This program provides a graphical interface for all the commands, allowing simple serial control of the DDS8m. A USB-to-Serial adapter is also available.*

NOTE:

For maximum interface speed, the parallel inputs do not have additional protection against ESD damage beyond that provided by the CMOS inputs (±2kV, Human Body Model. ±200V, machine model).

WARNING:

The byte parallel inputs are 3.3V CMOS compatible. Applying 5V logic signals to these inputs will permanently damage the DDS8m. If your system is 5V, it is suggested that VHC buffers powered by 3.3V be placed between the DDS8m and your system. You may use the 3.3V on pin 2 of P4 for this power (up to 50mA).

3.8 All of the inputs are 3.3V VHCMOS compatible and require:

V_{il} <= 0.4V

V_{ih} >= 2.7V

3.9 C_{in} on each pin is approximately 10pF (application cable capacitance not included). All the input pins are series terminated with a 47Ω resistor. It is recommended that a series termination resistor of 50-100Ω be used at each signal line source to prevent reflections and ringing. The exact value will be determined by your application circuitry and cabling.

3.10 Please refer to the timing diagram, Figure 2, and Parallel Control Timing, Table 6, for the details on setting frequency and phase when using the parallel interface.

3.11 **Internal Clock.** If you plan to use the DDS8m internal clock, verify that the clock select jumper wire (W1, see Figure 1) is in the INT position and that the External Clock Input is left unconnected (the jumper is a short piece of #28 AWG bare wire).

3.12 **External Clock**. If you are providing your own clock source, move the clock select jumper (W1, see Figure 1) to the EXT position. Apply your clock to the External Clock Input SMB. Note that phase noise and stability are now dependent upon your supplied clock. See specifications for signal levels required and acceptable frequency range.

3.13 The external clock can also be used with Kp=1 for direct connection to the DDS generator. With Kp=1, the PLL multiplier is disabled. Use this direct input, up to 300MHz, for optimum phase noise performance.

NOTE:

When using an external clock, frequency scaling of the "F" command may be required. Please see Operation, Section 4, for details.

3.14 **Signal Outputs.** There are three signal outputs on the DDS8m: Sine (Q), Cosine (I) and ACMOS/TTL. The Sine, Cosine and ACMOS/TTL are provided on SMB connectors on the board edge. Simply connect your 50Ω application cable to appropriate output. If you are not using the ACMOS/TTL output, it is suggested that it be disabled by sending the "A D" command for best system noise performance.

3.15 The DDS8m has a CLOCK OUT which can drive other DDS8m External Clock inputs. With no load, this output is a 1Vpp square wave at the clock oscillator or external clock frequency with a nominal output impedance of 50Ω. This output is used for daisy-chaining additional DDS8m from a single clock. This clock output may be used when multiple DDS8m are required to be synchronized. One DDS8m is then used as a master, using its internal clock. The secondary DDS8m, set for external clock

input, is then connected to the clock output on the master. All DDS8m connected in this way will remain phase synchronous. The absolute phase relationships will depend upon commands used, frequency output and delays between each unit. This output is usable up to approximately 50MHz.

3.16 Phase relationships in the Byte Parallel Control Mode are maintained by applying appropriate frequency and phase data to all units and then sending a single IOUD pulse to all units with all the DDS8m running from the same clock source.

3.17 **Mounting.** Six mounting holes are provided on the board. These holes are electrically connected to circuit common and may be used for shield connections. Clearance is provided for up to 3mm diameter screws. Please allow at least 3 mm clearance on the bottom side when mounting to a conductive chassis or case. Refer to Table 3 and Figure 1 for locations.

NOTE:

The DDS8m is cooled by convection. Verify that there is adequate free air flow around the board when mounting in an enclosure. Approximately four Watts are dissipated.

4.0 Operation

4.1 **Power on reset.** After power is applied, the DDS8m takes one second to initialize. Commands sent during this time will be ignored or may cause erroneous operation.

4.2 **Serial Operation.** After the DDS8m has been installed in the customer application system, all that is required for operation is to send the appropriate RS232 commands per Table 2. W3 (see Figure 1) must be installed before power-up for the serial mode to be recognized.

4.3 See Table 5 for Serial Firmware Modes of the DDS8m.

4.4 The user host computer software must properly format the serial commands. Incorrect formatting will result in an error code being returned. See Table 1 for a list of RS232 error codes.

4.5 For maximum interface speed, it is suggested that Echoing be disabled by the "E D" command. This will allow the host to send characters at a faster rate. Note that no flow control is provided. Depending upon your host, the DDS8m may not be able to keep up with serial characters. The DDS8m will respond with an "OK" for a correctly received data command. You will have to verify correct operation at your host rate.

4.6 If you are using an external clock, the value sent to the DDS8m during the "F" command must be scaled. The output frequency of the DDS8m when used with an external clock is given by:

$$F_{out} = (F_{command})*(F_{ext\ clk}/F_{int\ clk})$$

4.7 The nominal Internal Clock has a value of 28.1474976710656MHz. Best performance is obtained when the External Clock input times the Reference PLL multiplier (Kp) is close to the default value (281.475MHz; max. 300MHz).

4.8 For an example, suppose an external clock of 10.000MHz is used and an output of 1.544MHz is desired:

$$F_{command} = (1.544)*(28.1474976710656)/10.0$$
$$= 4.345973640413$$

4.9 The command then sent to the DDS8m for the 1.544MHz output, with a 10MHz external clock, will be (assuming Kp is unchanged):

```
f0 4.345973640413
```

NOTE:

You must account for your clock frequency error and calculation roundoff when using an external clock and the serial mode. Most hand calculators do not have enough digits to match the resolution of the DDS8m.

4.10 Since the resolution of the DDS8m is 48-bits, the typical fractional error for output frequencies in the MHz range will be less than $1x10^{-12}$, even when exact values are not possible. The Novatech Instruments, Inc. Model LPO30A can be used to lock to

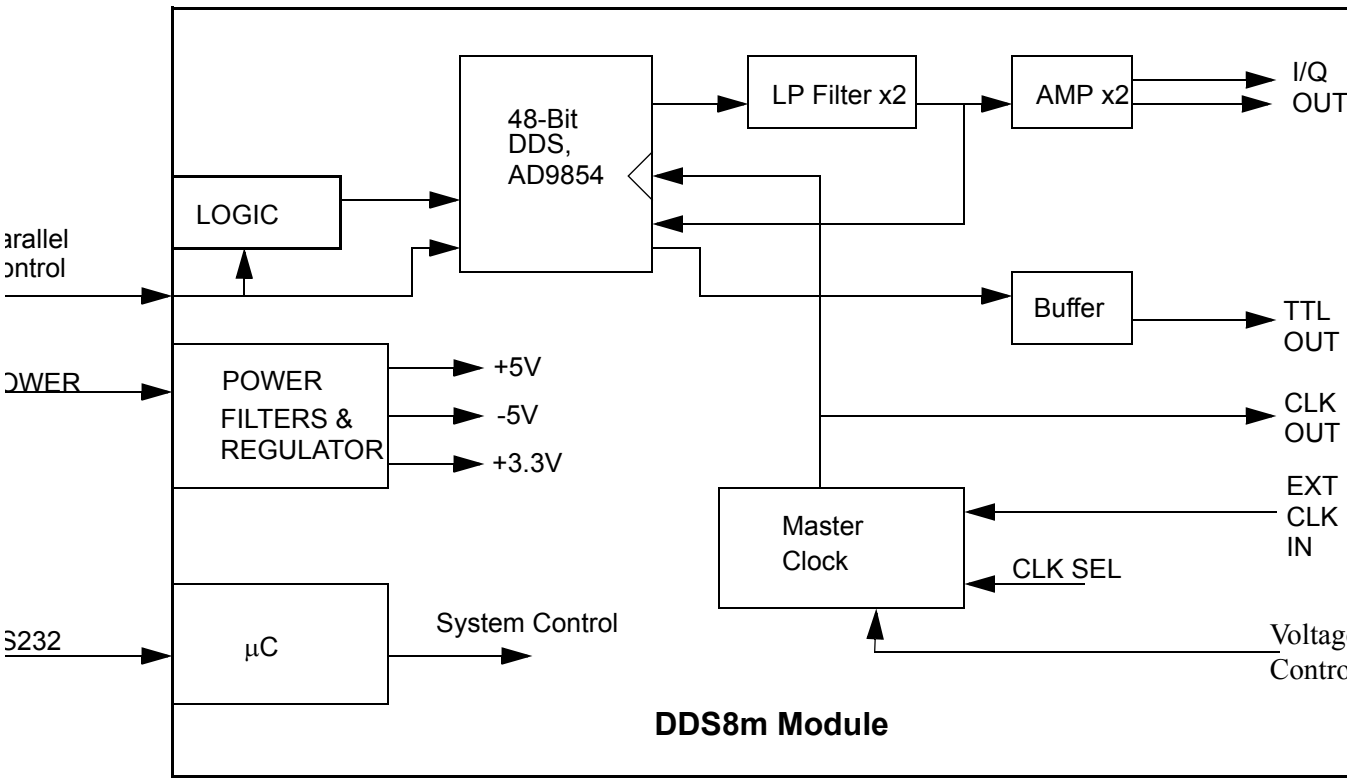


Figure 3.
Simplified System Block Diagram

Table 7: DDS-chip Internal Registers (MSB lowest address)

Address (Hex)	Function	Default Value (Hex)
00 to 01	Phase Adjust Register #1, 14-bits, bits 15, 14 don't care	00 00
02 to 03	Phase Adjust Register #2, 14-bits	00 00
04 to 09	Frequency Tuning Word Number 1, 48-bits	09 18 4e 72 a0 00
0a to 0f	Frequency Tuning Word Number 2, 48-bits	00 00 00 00 00 00
10 to 15	Delta Frequency Word, 48-bits	00 00 00 00 00 00
16 to 19	Update Clock, 32-bits	00 00 00 05
1a to 1c	Ramp Rate Clock, 20-bits, bits 23, 22, 21, 20 don't care	00 00 00
1d	4=CMP PD, 3=low, 2=QDAC PD, 1=DAC PD, 0=DIG PD	00
1e	6=PLL RNG, 5=BP PLL, 4-0=REF MULT	4a
1f	7=CLR ACC1, 6=CLR ACC2, 5=TRI, 4=QDAC, 3-1=MODE, 0=IOUD	00
20	6=BP INV SINC, 5=OSK EN, 4=OSK INT	40
21 to 22	Output Shape Key #1 Multiplier, 12-bits, bits 15, 14, 13, 12 don't care	0f ff
23 to 24	Output Shape Key #2 Multiplier, 12-bits, bits 15, 14, 13, 12 don't care	0f ff
25	Output Shape Key Ramp Rate, 8-bits	00
26 to 27	QDAC, 12-bits, 2's complement, bits 15, 14, 13, 12 don't care	0f ff

external references and create signals without fractional frequency error.

Typical Δf/f for External Clock of 10.0MHz

Kp	Desired Fout	Command	Δf/f
10	1.544MHz	f0 4.345973640413	$1.09x10^{-13}$
20	1.544MHz	f0 2.172986820206	$3.93x10^{-13}$
10	2.048MHz	f0 5.764607523034	$1.33x10^{-13}$
20	2.048MHz	f0 2.882303761517	$3.06x10^{-13}$

4.11 **Byte Parallel Operation (DDS8m only).** When the parallel mode is chosen, the operation of the DDS8m is completely dependent upon the user supplied interface circuitry. The on-board microprocessor and software are disabled in parallel operation. Therefore, no error conditions are detected or reported.

NOTE:

*The "**B**" command can be used to simulate the byte parallel control mode as it allows access to all internal registers. While not a real-time simulation, each "**B**" command functions as a parallel input by putting a data byte "**dd**" at an address "**aa**", and then pulses the WRB- and IOUD lines. This is the same procedure that a parallel control circuit would perform. Contact Novatech Instruments, Inc. for detailed information if you need application assistance.*

All modes and set up conditions for the Analog Devices AD9854 can be accessed by using the parallel interface or by using the "B" command. Please consult the AD9854 specifications for detailed operation.

Note that the DDS8m firmware modes are not identical to the AD9854 data sheet modes.

4.12 When using the default internal clock, 1LSB of the byte parallel mode frequency setting is equal to 1μHz.

4.13 As in the serial mode, the use of an external clock scales the frequency output of the DDS8m. Using the 10MHz example of the serial mode description (where $F_{setting}$ is the total binary value sent to the DDS8m):

$$F_{out} = F_{setting} * F_{ext}/F_{int}\ \mu Hz$$
$$F_{out} = 0.35527136788 * F_{setting}\ \mu Hz$$
$$F_{setting} = \text{Binary Value in DDS IC}$$

4.14 Note that values of $F_{setting}$ greater than 2^{47}-1 violate the Nyquist Theorem Limit for the DDS8m as it is a sampled data system.

4.15 The on-board Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO) can be adjusted approximately ±5ppm from nominal by applying a 0 to 5Volt signal on P3. Your voltage control must be capable of sourcing and sinking 0.5mA. The nominal unloaded voltage at calibration is 2.37Volts. This feature is useful for applications which require Phase Locking to external sources, using customer supplied circuitry.

4.16 For systems requiring locking to an external reference, the Model LPO30A can be used to generate an external reference for the DDS8m. The LPO30A can generate the required 28,147,497.6710656MHz external clock with a maximum error of 0.4μHz, or a fractional frequency error of $1.4x10^{-14}$, when locked to an external source.

4.17 For applications which require amplitude matching between the I and Q channels, the recommended method is to use the "Vx N" command to adjust the I or Q channel to match the other.

5.0 Theory of Operation

5.1 Please refer to the simplified System Block Diagram in Figure 3 for the following discussion.

5.2 At every cycle of the DDS8m master clock, the 48-bit DDS integrated circuit increments the phase of an internal register by a value determined by the frequency setting loaded into the on-chip registers. This digital phase value is converted to both sine and cosine amplitude levels and delivered to on-chip 12-bit digital-to-analog converters. The analog signals from these converters are filtered by two 7th-order elliptical low pass filters, amplified and sent to the Cos(I) and Sine(Q) OUT SMB receptacles.

5.3 The filtered cosine signal is also sent to an on-chip comparator converting the cosine level to a 3.3V ACMOS/TTL level signal which is then sent to the ACMOS/TTL OUT SMB receptacle. See specifications for output level details.

5.4 The frequency generated by the DDS IC is determined by the 48-bit frequency word loaded into the frequency register on the DDS8m. The output frequency is given by:

$$F_{out} = F_{setting} * Kp * F_{clock} / 2^{48} \text{ Hz}$$

Where: F_{clock} = 28,147,497.6710656 Hz (int.)
$F_{setting}$ = Binary value in DDS IC.
($F_{setting}$ ranges from 0 to 2^{47}-1)
Kp = PLL Multiplier (4 to 20, or 1)

This reduces to:

$$F_{out} = F_{setting}\ \mu\text{Hz}$$

for the internal (default) clock and the default PLL Multiplier (Kp=10) settings.

5.5 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the master clock frequency ($F_{setting}$ <= 2^{47}-1). While it is possible to generate an output near 50% of the clock, the distortion may be unacceptable. Therefore, the output is limited to approximately 40% of the system clock and steep output filters are provided on board: in this case 7th-order elliptical low pass filters.

5.6 If you are using an external clock and a Kp which give a clock substantially lower than the 281.47MHz default internal clock, you may need to filter the Sine and Cosine Outputs to obtain acceptable distortion for your application. For best performance, set the corner frequency at 40% or less of your external clock frequency times Kp. The lower your filter as a percentage of your clock frequency, the lower the distortion.

NOTE:

Since filtering occurs before the signal is level shifted to ACMOS/TTL, the ACMOS/TTL output may be erratic or distorted when using low clock frequencies. If you require an ACMOS/TTL level signal when using low clock frequencies, it is recommended that you use an external comparator/ level shifter connected to the output of your external filter. Contact Novatech Instruments, Inc. if you require application assistance.

5.7 For example, if you are using a 10MHz external clock, with the default reference multiplier (Kp) of 10, then the internal clock is 100MHz. An optimal filter for this frequency would then be approximately 40MHz (40% of 100MHz).

5.8 In amplitude modulation (the "Z" command), the modulation frequency is derived from the microcontroller clock and is asynchronous to the carrier. The modulation signal is unfiltered and is a stepwise approximation to a sine wave.

6.0 PERFORMANCE TEST

6.1 Install the DDS8m as directed in the Serial Operation part of Section 3. Connect your host controller and operate the DDS8m per Section 4. The test limits assume a stable environment of 18-28^{o}C.

6.2 If you are using a byte parallel controller, you will have to adjust the commands to match your controller.

6.3 The performance test detailed below verifies each functional block on the DDS8m.

NOTE:

Allow the DDS8m to warm up for at least 15 minutes before performing any measurements. For best results, the DDS8m should be verified in its installed environment.

6.4 See Table 8 for a list of recommended test equipment to perform the following measurements.

Table 8: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	300MHz, 50Ω	Tektronix TDS3032B
RF Probe	100kHz-100MHz	Tektronix P6420 or HP34301A
DMM	ACrms, dB	HP34401A
50Ω Termination	50Ω, ±1%	Tektronix 011-0049-01
Frequency Counter	120MHz	HP53132A
Counter Time Base	<±0.1ppm	Novatech Instruments Model 2960AR

6.5 **Verify Frequency Accuracy.** To verify the frequency of the DDS8m, set the output sequentially to each value in Table 9. Connect the recommended frequency counter set to 50Ω termination and 1Hz resolution. Verify the limits show in Table 9. Test Sine (Q) Out, Cosine (I) Out and ACMOS Out to verify functionality of all outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. (LSD = **L**east **S**ignificant **D**igit on counter).

Table 9: Frequency Test Points

Frequency	Tolerance
100 kHz	±0.15Hz ±1 LSD
1 MHz	±1.5Hz ±1 LSD
10 MHz	±15Hz ±1 LSD
30 MHz	±45Hz ±1 LSD
50 MHz	±75Hz ±1 LSD
99 MHz	±150Hz ±1 LSD

6.6 **Sine (Q) Out Amplitude Verification.** Set the frequency of the DDS8m to 100kHz. Connect the DDS8m to the DMM through a 50Ω feedthrough termination. Set the DMM to AC Volts. Verify a reading of 0.5Vrms ±0.05Vrms. Remove the 50Ω termination. Verify an amplitude of 1.0Vrms ±0.1Vrms. Repeat for the I output.

6.7 **Level Command Test.** Leave the output frequency set to 100kHz. Send the commands "`Vi 2048`" and "`Vq 2048`". Verify that the amplitude on the I and Q channels decrease by half. Send the "`R`" command to reset the levels before performing the next tests.

6.8 **Output Flatness Verification.** Verify that the Sine (Q) Out is flat with frequency by performing the following test: Connect an RF probe to the DDS8m terminated with a 50Ω feedthrough termination. Connect the output of the RF probe to the DMM, set to DC Volts. Set the output of the DDS8m to 30MHz. Select dB on the DMM.

6.9 Set the DDS8m to the values of Table 9. Verify that the DMM reading is 0dB ±3dB.

6.10 Repeat the output flatness verification test for the Cosine (I) output.

6.11 **ACMOS/TTL Verification.** Using a short 50Ω coaxial cable, connect the ACMOS/TTL output to the recommended oscilloscope set for 50Ω termination. Using the values of Table 9, verify that the output duty factor ranges from a minimum of 45% high and 55% low to a maximum of 55% high and 45% low.

6.12 Set the frequency to 10kHz. Change the termination from 50Ω to 1MΩ on the oscilloscope. Verify that the 50Ω amplitude is 1/2 that of the 1MΩ amplitude, ±10%.

6.13 **Clock Out Verification.** Connect a frequency counter through a 50Ω feedthrough termination. Verify a frequency reading of 28,147,497.6711 Hz ±28.15Hz. Using the oscilloscope, verify a peak-to-peak amplitude of approximately 1 Volt.

6.14 **FSK Test.** (DDS8m only) Setup an FSK mode (see Appendix A) with the following commands:

```
M 0
F1 1.000
F2 10.000
M 1
```

6.15 Connect a jumper test lead from P4 pin 1 to P4 pin 8. Verify a frequency of 1.000MHz (± tolerance of Table 9).

6.16 Move the jumper test lead from pin 1 to pin 2. Verify a frequency of 10.000MHz (± tolerance from Table 9).

6.17 This concludes the verification test of the DDS8m.

7.0 CALIBRATION

7.1 The DDS8m has only two adjustable components: Y2, frequency; and R52, output amplitude. Calibration should be performed only if the DDS8m fails the performance test or if the unit has been repaired. Routine adjustments are not recommended nor generally required. This procedure assumes that the DDS8m has failed the performance test or has been repaired.

7.2 The adjustments shown are set to 1/2 the specification limit values.

NOTE:

Allow the DDS8m to warm up for at least 15 minutes before performing any adjustments. For optimum performance the DDS8m should be calibrated in its installed environment.

7.3 **Frequency Adjust, Y2.** Set the output of the DDS8m to 10.000000MHz. Connect the Cosine (I) Output to your frequency counter set for 50Ω termination. Adjust Y2 using a non-metallic adjustment tool for 10.000000MHz, ±7.5Hz.

7.4 **Amplitude Adjust, R52.** Set the frequency to 100kHz. Connect the Cosine (I) Output to the DMM set for AC Volts. Do not use a 50Ω termination. Adjust R52 for 1.00Vrms ±0.05Vrms. This completes the calibration of the Model DDS8m.

8.0 Appendix A. DDS8m Mode Details.

NOTE:

The examples assume default values are unchanged.

8.1 **Mode 0.** Mode 0 is a single frequency output. For simple operation, only F0 need be set.

8.2 **Mode 1. F**requency **S**hift **K**eying. In this mode Pin 8 of the parallel interface connector selects between F1 and F2 based upon its logic level. A logic 1 (3.3 Volts) selects F2, while a logic 0 (0 volts) selects F1. The change in frequencies is phase continuous. FSK rates of up to 15MHz can be used.

8.3 To program Mode 1 send the following commands:

```
M 0
F1 xx.xxxx
F2 yy.yyyy
M 1
```

8.4 Connect your FSK control signal to Pin 8 of the connector, P4. Make sure your signals are 3.3 Volt logic levels. If left unconnected, pin 8 is pulled up through a 10kΩ resistor to +3.3 Volts (logic 1), selecting F2.

8.5 **Mode 2.** Ramped FSK. In Mode 2, the output frequency is continuously ramped from F1 to F2 to F1 in steps of Fd with dwell times of DT. Figure A1 gives a visual representation.

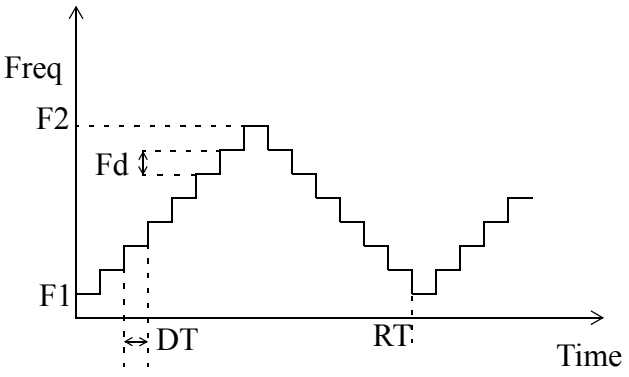


Figure A1: Mode 2 Timing.

8.6 It will be necessary to set Tr in Mode 2 if you wish to align the trigger pulse on pin 10 of P4 to the frequency updates. See description which follows.

8.7 To use the trigger pulse you must set F1, F2 and Fd to produce an integer number of steps from F1 to F2. The proper value for Tr is then given by:

Tr = N*(Td+1) - 1
where
N = (F2-F1)/Fd

8.8 Note that DT= (Td+1)/(Fclk*Kp) and RT= 2*N*DT. For the default clock and Kp the minimum DT is approximately 3.55ns.

8.9 Tr must be an integer from 5 to 4294967295 (2^{32}-1). If the solutions for N and Tr are not exact integers, the location of the timing pulses will "slide;" that is, not remaining synchronous, with respect to the changes in frequency.

8.10 Note further that the parameter Tr is not necessary in Mode 2 unless you plan to use the trigger pulse. If you do not need a trigger pulse, then you can ignore Tr.

8.11 Mode 2 example. Assume F1=1MHz, F2=51MHz, Fd=0.25MHz and Td=1000. This gives:

N = (F2-F1)/Fd = 200
so
Tr = N*(Td+1) - 1 = 200199

8.12 The serial commands sent to the DDS8m would then be:

```
M 0
F1 1.0
F2 51.0
Fd 0.25
Td 1000
Tr 200199
M 2
```

8.13 The DDS8m immediately begins generating the requested signal.

8.14 **Mode 3**. Chirp. Mode 3 is set to default to a "sawtooth" frequency output. That is, the frequency will ramp from a starting frequency, F1, in steps of

Fd at a rate of DT until timed out by RT. In Mode 3, Tr must be set as it controls the time the output frequency returns to F1. See Figure A2 below for a visual representation.

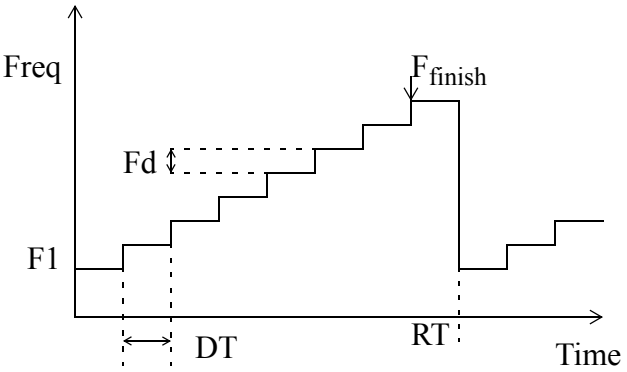


Figure A2: Mode 3 Timing.

8.15 The relationships among the various parameters used in Mode 3 are:

F_{out} = F1 + Fd*(Time/DT), (Time/DT) must be an integer.

DT = $(n_{td}+1)/(F_{clk}*Kp)$ Kp=PLL MULT

RT = $2*(n_{tr}+1)/(F_{clk}*Kp)$

$n_{tr,td}$ = value input at Tr and Td commands.

8.16 IOUD will be set to an output (pin 10 of P4) and have a period of RT with a nominal high pulse width of 8 system clock cycles: $8/(F_{clk}*Kp)$.

8.17 For an example of Mode 3, consider the desire to sweep to 18.33MHz starting from 16.66MHz in 1.5ms with as many steps as possible to simulate a linear ramp. Assume the default clock for this example.

NOTE:

Pin 8 of the parallel interface connector (P4) must be held "LOW" for Mode 3 to function.

8.18 **Step 1:** Calculate Td. Since we want the most number of steps, use the smallest non-zero Td possible (1 to 2^{20}-1) or 1. This will give a value of 7.1054ns per step, allowing 211106 steps in 1.5ms.

8.19 **Step 2:** Find Fd. Fd = (F_{finish}-F1)/(Steps) or 7.911Hz. Since the Fd command takes 1μHz steps a value of 0.000007910718 would be entered.

8.20 **Find Tr:** Tr is the repeat time, in this example 1.5ms. So Tr = 211106. Note that if Tr is not set for the exact solution, the frequency ramp will either be stopped early or continue past F_{finish}. In Mode 3, Tr is a controlling constant.

8.21 The commands sent to the DDS8m would then be (assuming serial control):

```
M 0
F1 16.66
Fd 0.000007910718
Td 1
Tr 211106
M 3
```

8.22 The DDS8m immediately begins generating the requested signal.

8.23 **Mode 4. B**inary **P**hase **S**hift **K**eying. In this mode, Pin 8 of the connector, P4, selects between P1 and P2 based upon its logic level. A logic 1 (3.3 Volts) selects P2, while a logic 0 (0 volts) selects P1. The output frequency remains constant at F1. BPSK rates of up to 15MHz can be used.

8.24 To program Mode 4 send the following commands:

```
M 0
F1 xx.xxx or F0 xx.xxx
P1 ppppp
P2 qqqqq
M 4
```

p, q from 0 to 16383

8.25 Connect your BPSK control signal to Pin 8 of the connector. Make sure your signals are 3.3 Volt logic levels. If left unconnected, pin 8 is pulled up through a 10kΩ resistor to +3.3 Volts (logic 1), selecting P2.

8.26 **Custom Modes**. The DDS8m can be programmed by using the "B" command to perform many other outputs. Those listed above are preprogrammed for ease of use. Either the parallel port or

the "B" command can be used to gain complete control over the on-board DDS ASIC. Contact Novatech Instruments, Inc. for further application assistance.

8.27 **Special Modes.** Novatech Instruments, Inc. has implement other modes as specials. Mode 8, along with some customer supplied external hardware, implements a "chirped-pulse" function. Mode 9 performs an FSK function with a return to zero phase and zero frequency. If you are interested in these modes, please contact the factory.

9.0 Appendix B: DDS8p.

NOTE:

This appendix covers the Model DDS8p, which has high-speed 48-bit parallel binary frequency and 14-bit parallel binary phase interfaces in addition to the serial interface of the standard model. Please refer to the DDS8m section of this manual for details on basic operation and installation.

9.1 DDS8p Specifications (in addition to DDS8m):

9.2 **OUTPUT:** The output frequency range is 100Hz to 120MHz (Sine, Cosine and ACMOS) in 1μHz steps per LSB on the parallel interface (internal clock and default settings).

9.3 **BINARY PARALLEL CONTROL.** The Parallel interface is on a 60-pin header for frequency (backwards compatible with the DDS8m/03 and PAR-48) and on a 24-pin header for phase control (see below for pinout and timing).

9.4 **SERIAL CONTROL.** The RS232 port on the DDS8p board can be enabled by setting W3, see details below. (Only Mode 0 can be used during serial operation on the DDS8p.)

9.5 **SIZE:** 5.1 inches by 3.6 inches by 1.0 inch high (129.5mm by 91.4mm by 25.4mm), not including connectors.

9.6 **CONNECTORS:** 30x2 header with 0.025inch (0.635mm) square posts on 0.1inch (2.54mm) spacing for Frequency and control signals; 12x2 for Phase. A 3-pin header is provided for power (same as DDS8m).

10.0 DDS8p Installation Notes

10.1 The installation of the DDS8p is similar to the Model DDS8m with the exception of the binary parallel interface connections. Please refer to the DDS8m manual for basic installation notes.

10.2 The default initialization values (the output after a power-up but before a LOAD- pulse has been issued) can be set by putting the DDS8p into RS232 serial mode. This is accomplished by installing W3, cycling power and using the serial commands detailed in the DDS8m manual. Once the desired settings are established, use the 'SAVE' command to store the values. Remove W3 and again cycle power. The DDS8p will then initialize with the values set by the 'SAVE' command. Please note that the DDS8p implements only **Mode 0** of the DDS8m. Parallel operation and serial operation are mutually exclusive. In serial mode, the timing of the standard DDS8m module applies.

10.3 The on-board dip switch (S1, see component placement diagram) is used to set the value of Kp used and for EXT/INT Clock Select position. When pushed toward the board edge, the internal VCTCXO is selected. When set away from the board edge, the external clock is used. The internal source is always used for internal timing on the DDS8p board. Default setting is for the internal clock.

WARNING:

Use extreme care during installation and removal of cabling to the DDS8p. Do not unduly flex the board, which could result in damaged surface-mounted components.

10.4 See signal description, timing diagram, timing table and signal notes below for operation of the parallel adapter connectors.

11.0 Parallel Input Requirements

NOTE:

The parallel inputs do not have additional protection against ESD damage beyond that provided by the CMOS inputs (±2kV, Human Body Model. ±200V, machine model).

11.1 The inputs on the DDS8p are both 3.3V and 5.0V CMOS logic tolerant. The BUSY- output is 3.3V VHCMOS logic.

11.2 All of the inputs, **FS0-47, LOAD-** and **IOUDm-**, are VHCMOS compatible and require: V_{il}<=0.3*V_{cc} (0.9 volts max) (1.0 volts nominal) V_{ih}>= 0.7*V_{cc} (2.5 volts min) (2.3 volts nominal)

NOTE:

Using TTL input signals may not provide acceptable noise margins depending upon your application circuitry; 3.3V VHCMOS logic levels are suggested.

11.3 C_{in} on each pin is approximately 10pF (application cable capacitance not included). All the input pins are pulled to V_{cc} (nominally 3.3v) via pull-up resistors. It is recommended that a series termination resistor of 50-100Ω be used in each signal line to prevent reflections and ringing. The exact value will be determined by your application.

12.0 DDS8p Signal Descriptions

12.1 **FS0** through **FS47** are the 48 binary data bits presented to the internal DDS frequency output register. The frequency output for the default values of Kp (10) and the internal clock (28.147...MHz) will have 1μHz of resolution per LSB. Since there is no error checking of the user input, care must be taken to ensure that the binary value does not select a frequency output greater than approximately 120MHz to maintain acceptable filtering performance.

12.2 **PS0** through **PS13** are the 14 binary data bits presented to the internal DDS phase offset register. Note that the Sine and Cosine outputs are always a nominal 90° apart. This phase setting offsets the DDS8p from an arbitrary reference (see IOUDm- below). The phase offset is N*360°/16384 or N*π/8192, were N is the binary value of PS0 through PS13 (maximum value 16,383).

12.3 **BUSY-** is a VHCMOS compatible ***output*** with: V_{oh}>=3.0V (I_{load}<=-100μA) V_{ol}<=0.2V (I_{load}<=100μA)

12.4 BUSY- going HIGH indicates that all parallel data has been loaded into the DDS circuitry and the new frequency will become stable approximately 170ns later. Please refer to timing diagram for details.

12.5 BUSY- has a series resistance of approximately 500Ω to prevent damage due to accidental shorts. If this output is used for handshaking, be sure to account for capacitive loading on this signal.

12.6 Please refer to the timing diagram (Figure B1) and table (Table B1) below for the details of setting frequency and phase on the binary parallel interface.

12.7 **LOAD-** going LOW is used to signal the on-board circuitry to load a new frequency into the DDS registers. The negative edge of LOAD- is latched and presented on the BUSY- line. The negative edge also transfers data from the user application connection to internal latches. Data must be stable at least 10ns before the negative edge of LOAD-. During BUSY-, all appropriate registers on the DDS8m are programmed and, upon completion of the loading process (BUSY- returning HIGH), a new frequency is available at the output after approximately 170ns of pipeline delay. The timing of BUSY- returning HIGH may have up to ±36ns of ambiguity due to timing synchronization internal to the parallel interface board.

NOTE:

The ACMOS output may be erratic when pulsing the output due to internal time constants (T_{zd}). If an ACMOS signal is required in pulse applications, it is recommended that the customer consider external level shifting circuitry. Best pulse performance is obtained from the 'Q' Channel. Consult the factory if you need a smaller T_{zd}.

Figure B1: DDS8p Parallel Input Timing Diagram (Not to Scale)

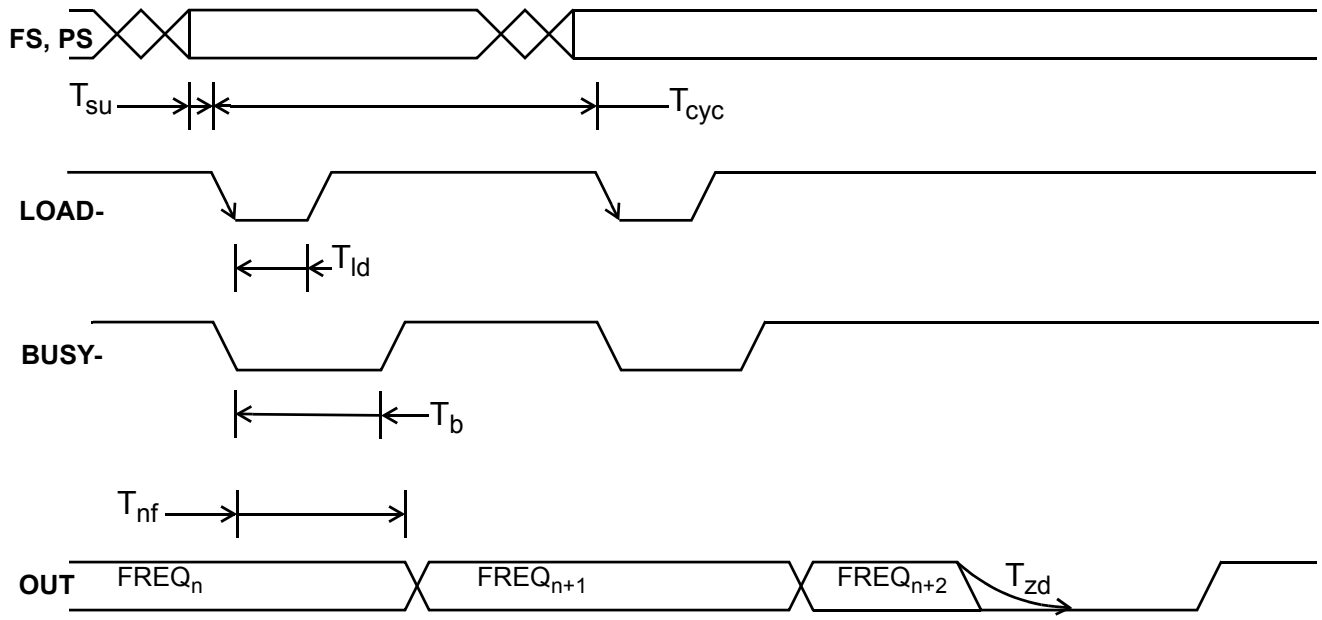


Table B1: Timing, Internal Clock, default Kp.

Parameter	Name	Min	Max	Notes
T_{su}	Binary Data Setup	10ns		Binary Data Stable before LOAD-.
T_{ld}	Load Pulse Width Low	25ns		Minimum Load pulse width.
T_b	Busy Time		430ns	Busy- is LOW for internal data transfer.
T_{nf}	New Frequency Time		600ns	New frequency on output.
T_{zd}	Zero Decay Time		100μs TYP	Time for Output to decay to ±100mV (for zero frequency setting).
T_{cyc}	Load cycle time	600ns		Cycle time before next LOAD- time.

12.8 **RES-** is the reset signal. When LOW all the circuitry on the DDS8m and the DDS8m parallel adapter is reset. Upon returning HIGH, the DDS8p will initialize in approximately 1sec and output a frequency of 10MHz (internal clock and default Kp).

12.9 If the serial mode was used to save a different startup frequency, then the user-saved values will be used after a reset or power cycle. Kp is read from the switch, S1, only upon a reset or power cycle.

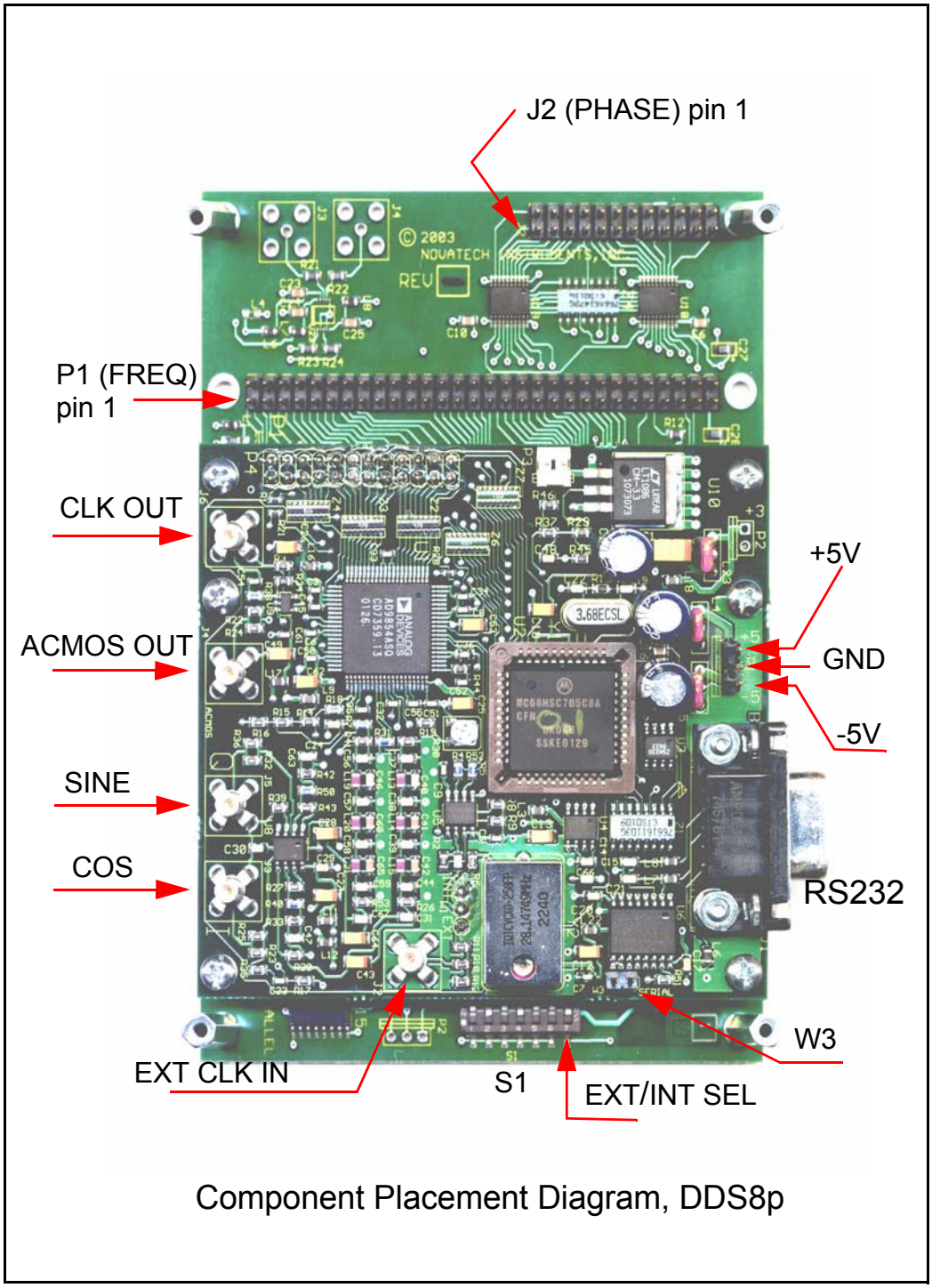
12.10 **IOUDm-** is a master I/O update signal. This signal can be used to synchronize multiple DDS8p. Normally left open (pulled HIGH on board), IOUDm- can be held LOW during a frequency/ phase LOAD- and BUSY- time. Upon release to OPEN or HIGH, all DDS8p connected to the same line will transfer the loaded data into the active registers on the DDS ASIC. This will start each DDS8p board output at the same time. If used with a common external clock, all of the common connected DDS8p will then remain phase synchronous.

Table B2: P1, Frequency Data and Control Connector. DDS8p

P1 Pin Number	Function	P1 Pin Number	Function
1	Frequency Select 1 (FS1)	2	Frequency Select 0 (FS0) (LSB)
3	FS3	4	FS2
5	FS5	6	FS4
7	FS7	8	FS6
9	FS9	10	FS8
11	FS11	12	FS10
13	FS13	14	FS12
15	FS15	16	FS14
17	FS17	18	FS16
19	FS19	20	FS18
21	FS21	22	FS20
23	FS23	24	FS22
25	FS25	26	FS24
27	FS27	28	FS26
29	FS29	30	FS28
31	FS31	32	FS30
33	FS33	34	FS32
35	FS35	36	FS34
37	FS37	38	FS36
39	FS39	40	FS38
41	FS41	42	FS40
43	FS43	44	FS42
45	FS45	46	FS44
47	FS47 (MSB)	48	FS46
49	Circuit Common (GROUND)	50	BUSY- ***(OUTPUT)***
51	LOAD-	52	Circuit Common (GROUND)
53	nc	54	IOUDm- (leave open)
55	nc	56	nc
57	RES- (must be OPEN on REV- assemblies)	58	nc
59	Circuit Common (GROUND)	60	Circuit Common (GROUND)

Table B3: J2, Phase Data. DDS8p

J2 Pin Number	Function	J2 Pin Number	Function
1	Phase Select 1 (PS1)	2	Phase Select 0 (PS0) (LSB)
3	PS3	4	PS2
5	PS5	6	PS4
7	PS7	8	PS6
9	PS9	10	PS8
11	PS11	12	PS10
13	PS13 (MSB)	14	PS12
15	nc	16	***Do Not Connect***
17	nc	18	nc
19	nc	20	nc
21	nc	22	nc
23	Circuit Common (GROUND)	24	Circuit Common (GROUND)



Component Placement Diagram, DDS8p

13.0 Hardware Mounting:

13.1 The DDS8m synthesizer module is attached to the DDS8p parallel adapter board using 6 aluminum spacers and 12 screws. These must remain undisturbed. There are 6 free mountings holes with clearance for 3mm or #4 screws. The mounting hole pads are connected to Circuit Common (ground). It is suggested that all 6 positions be used to attach the DDS8p board into the application. Please leave approximately 3mm clearance spacing from the bottom of the board.

14.0 Theory of Operation

14.1 The DDS8m core circuitry is a Model DDS8m and the theory of operation of Paragraph 5.0 applies. The DDS8p binary parallel adapter board consists of a set of latches and a state machine to load all the binary parallel data within 600ns.

15.0 Binary Parallel Performance Test

15.1 The testing of the DDS8p is the same as the DDS8m, except the control is dependent upon the customer supplied control circuitry.

16.0 Calibration.

16.1 The DDS8p has no additional calibration requirements from that of the DDS8m. Please refer to Section 7 for calibration.

WARRANTY

NOVATECH INSTRUMENTS warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS.

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