INSTRUCTION MANUAL

Precision 350 MHz Synthesizer

Model 425A

Table of Contents

1.0 DESCRIPTION

1.1 The Model 425A is a 48-bit Direct Digital Synthesized (DDS) Signal Generator in a small shielded table top case with an asynchronous serial control port (RS232). The 425A provides sine wave, LVDS and LVCMOS output signals, which can be set from 250 kHz to 350 MHz in steps of 10 μHz per LSB when using the internal VCTCXO clock

1.2 Relative phase is adjustable over the same interface with 14-bits of resolution. Amplitude can be fine trimmed over a 10-bit range from approximately 0.14 to 0.50 V_{rms} into 50 Ω.

1.3 The LVCMOS output is optimized for frequencies up to 125 MHz and, when used with its programmable divider, provides square wave clock signals down to lower than 2 Hz.

1.4 The 425A can also be used with an External Clock or Reference input. The external source can either be a 10.0 MHz reference, which is phase-locked internally, or a direct input of 250 to 1000 MHz. When used with the same external clock source, multiple 425A remain phase synchronous.

2.0 SPECIFICATIONS

2.1 OUTPUTS

TYPES: Sine, LVDS and LVCMOS simultaneously.
IMPEDANCE: 50 Ω. (100 Ω differential for LVDS)
RANGE: 250 kHz to 350 MHz with 10 μHz resolution (internal clock).
SINE AMPLITUDE: full scale approximately +7 dBm (0.50 Vrms) into 50 Ω load. Settable from 0.14 to 0.50 V_{rms} by the "V0" command. (14-bit DAC). ±3dB referenced to amplitude at 100 MHz.

2.2 LVCMOS AMPLITUDE

V_{OL}<0.5 V, V_{OH}>2.0 V into a series-terminated load.
$T_{r,f}$ <2.5 ns. Duty Factor: 40-60% (divider off). 50 Ω.
Programmable 16-bit divider with a selectable /2 prescaler allows LVCMOS frequencies below 2 Hz. (LVCMOS optimized for frequencies <= 125 MHz)

2.3 LVDS AMPLITUDE

Meets EIA-644A specifications when terminated into a 100 Ω differential load (driver: SN65LVDS100, or equivalent).

2.4 CONTROL

Output frequency (48-bits), phase (14-bits), CMOS divider, and amplitude scaling (10-bits) are controlled by a serial port. Settings can be saved in EEPROM.

2.5 ACCURACY AND STABILITY

Accuracy: < ±1.5ppm at 10-40 ^{o}C. Stable to an additional ±2ppm per year, 18-28 ^{o}C.

2.6 EXTERNAL CLOCK/REFERENCE IN

Direct external clock frequency range of 250 to 1000 MHz or locked to a 10.0 MHz (±0.01%) reference. The 425A specifications depend upon the quality of this signal.
Input Level (50 Ω.)**:**
10 MHz Reference: 0.75-1.25 Vrms Sine or LVCMOS Square Wave.
External Clock: -3 to +6 dBm sine wave.

2.7 SPECTRAL PURITY (Typical, 50 Ω load, int. clock)

Phase Noise:<-140 dBc, 10 kHz offset, 10 MHz out.

Spurious:	<-70 dBc below 10 MHz
	<-60 dBc below 50 MHz
	<-55 dBc below 150 MHz
	<-45 dBc below 350 MHz
Harmonic:	<-65 dBc below 1 MHz
	<-60 dBc below 10 MHz
	<-55 dBc below 25 MHz
	<-45 dBc below 50 MHz
	<-40 dBc below 150 MHz
	<-25 dBc below 350 MHz

2.8 POWER REQUIREMENTS

+4.75 to +5.25 V @ <750 mA. 2.5 mm center-positive connector on rear panel. AC line (country dependent) adapter provided.

2.9 SIZE

39 mm H, 107 mm W, 172 mm L, not including connectors.

2.10 CONNECTORS

BNCs for SINE Out, LVCMOS Out, LVDS out, REF IN. 2.5 mm center positive barrel connector for Power. DE9 for serial control.

3.0 HARDWARE INSTALLATION

3.1 **Power Connection.** Figure 1, shows the rear panel of the 425A. The required power of +5 Volts DC is applied through a 2.5mm center positive barrel connector.

Figure 1: Rear Panel

3.2 The quality of your power supply may affect the performance of the 425A. The supply should be free of ripple and noise (typically <50 mV). Even though extensive filtering is used on the 425A board, a quiet and well regulated power supply will ensure optimum performance. If power supplies, other than the Novatech Instruments provided one, are used, please verify that your system noise requirement is met.

3.3 **Internal Clock.** If you plan to use the 425A internal clock, which is the default mode, no setup action is required. The on-board VCTCXO is multiplied in a phase-locked loop (PLL) to generate the internal master clock for the DDS ASIC.

3.4 **External Clock**. There are two customer-supplied clock modes. One (external reference select, "`C r`") uses an internal PLL to multiply an external 10.0 MHz reference to provide a 940.0 MHz master clock. The other mode (external clock select, "`C e`") allows a 250 to 1000 MHz direct input. In this mode, the PLL is disabled and the customer clock is directly used as the master clock.

3.5 If you are providing an external clock or external reference, apply your signal to the **REF IN** BNC connector on the rear panel. Carefully observe the amplitude requirements for each mode. Note that phase noise and stability of the 425A are dependent upon your supplied clock. Send the appropriate clock select command to enable your input. This automatically configures the internal clock circuitry to generate the correct master clock.

3.6 Unless your external clock is an exact binary multiple, non-fractional frequency steps will not be possible, and your frequency settings will need to be scaled. See Section 4.0, Operation, for scaling information.

NOTE:

Consult Novatech Instruments if you require locking to an external 10.00 MHz standard without round-off.

3.7 **Serial Port Interface Installation.** The 425A is controlled by using an asynchronous serial port (RS232). Direct connections can be made from most PCs using a 9-pin monitor extension (male to female) cable or by using a USB to RS232 (DE9) adapter. The rear panel connector is a 9-pin female.

3.8 If you are using a different computer, terminal or other control source, please note that the data **TO** the 425A is on pin 3; the data **FROM** the 425A is on pin 2 and the **COMMON** return is on pin 5. Set your host to 19.2 kBaud, 8 bits, 1 stop bit, no parity and no hardware flow control.

3.9 **Signal Outputs.** There are three signal outputs on the 425A: one channel each of Sine, differential LVDS and LVCMOS. The outputs are provided on front panel BNC receptacle connectors. Simply connect your application cables to appropriate output. The LVDS output requires 100 Ω differential termination at the destination (internal driver: SN65LVDS100 or equivalent). All the outputs are at the same frequency, unless the divider (D0 and PR) commands have been issued. The LVCMOS output frequency depends upon the divider and prescaler settings.

3.10 See Figures 3 and 4 for typical termination of the LVDS and LVCMOS signals.

NOTE:

The LVCMOS signal is disable by default. Use the "`A e`" command to enable it.

Serial Command	Function
`F0 xxx.xxxxxxxxxxx`	Set Frequency of output in MHz to nearest 10 μHz. Decimal point required.
`P0 N`	Set relative **P**hase of output sinewave. N is an integer from 0 to 16383. Phase is set to N*360°/16384 or N*2π/16384 radians. This is useful when multiple Model 425A are running from the same clock source.
`E x`	Serial echo control. x=D for Echo **D**isable, x=E for Echo **E**nable. Disable echo for maximum serial port speed.
`C x`	Select clock source. x=E for **E**xternal 250 MHz to 1000 MHz direct input; x=R for 10.0 MHz **R**eference; x=I for **I**nternal temperature compensated reference. The quality of the external reference affects the specifications of the 425A. The "`F0`" command requires scaling (see manual) for clocks other than the internal oscillator.
`R`	Reset. This command resets the 425A. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
`CLR`	Clear. This command clears the EEPROM valid flag and restores all factory default values.
`A x`	x=E for LVCMOS **E**nable, x=D for LVCMOS **D**isable. Default setting is "D."
`D0 N`	Set **D**ivider value on LVCMOS output. N is an integer from 0 to 65535. The output frequency set by the "`F0`" command is divided by N+1 before being sent to the LVCMOS driver.
`PR x`	x=E for Enable Prescaler, x=D for Disable Prescaler. When enabled, the frequency set by the "`F0`" command is divided by 2 before entering the LVCMOS divider specified by the "`D0`" command. This allows a maximum divide integer of 131072.
`S`	**S**aves current state into EEPROM and sets valid flag. The saved state is used as the initial values upon next power up or reset. Use the "`CLR`" command to return to default values.
`QUE`	Return present frequency, phase and status. Returns a character string of all internal settings.
`M N`	**M**ode command. Mode '`M 0`' is single tone. (Only Mode 0 is implemented at software Rev 1.5.)
`V0 N`	Set **V**oltage level of output. In default, the amplitude is set to the maximum of approximately 0.5 V_{rms} (+7 dBm) into 50 Ω. N can range from 0 to 1023 (no decimal point allowed). Voltage level is scaled (multiplied) by: ***0.27 + 0.19*N/264*** If N >1023, the command is ignored and the level remains at its previous setting (approximately 0.14 V_{rms} to 0.50 V_{rms}).
`I x`	Set the **I**/O update pulse method. If x=a, then an I/O update is issued **a**utomatically at the end of each serial command (default). If x=m, then a **m**anual I/O update pulse is expected to be sent by a subsequent '`I p`' command.
B aabb[cc[dd[ee[ff[gg[...]]]]]]]	This **B**yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the instruction word "`aabb`". Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed.

4.0 Operation

4.1 **Power on reset.** After power is applied, the 425A takes approximately 300 ms to perform its initialization sequence. Any communication during this time will be ignored or may cause erroneous operation.

4.2 Specifications are met within 15 minutes of power-up in stable environment.

4.3 After the 425A has been installed in the customer application system, all that is required for operation is to send the appropriate data.

4.4 Serial commands are shown on the previous page. The commands consist of a one or two character alpha-numeric mnemonic separated from the operand by a space. Some commands do not have an operand, so the space is not necessary.

4.5 To facilitate use with various systems, the commands can be terminated by a line feed (LF), carriage return (CR) or any combination.

4.6 The user host hardware must properly format the asynchronous serial port data. Incorrect formatting will result in erroneous or erratic operation. See Table 1 for Serial Error Codes. Not all error codes are used in all versions.

Table 1: Serial Error Codes

Error Code	Meaning
`OK`	Good command received (not sent for R, CLR and QUE)
`?0`	Unrecognized Command
`?1`	Bad Frequency
`?2`	Bad AM Command
`?3`	Input line too long
`?4`	Bad Phase
`?5`	Bad Time
`?6`	Bad Mode
`?7`	Bad Amp
`?8`	Bad Constant
`?f`	Bad Byte

4.7 If you are using an external clock, the frequency value sent to the 425A command must be scaled.

4.8 The nominal Internal Clock has a value that produces a even step size of 10.0 μHz. Thus a scale factor is necessary to determine your exact output frequency when using external clock sources. For example, to obtain 10 MHz output when using a 10 MHz reference (940.0 MHz internal master clock), your frequency setting would be:

$F_{setting} = F_{desired}*0.998138215286$ MHz

$F_{setting} = 9.98138215286$

send: `F0 9.98138215286`

4.9 When used with an external clock of 250 MHz to 1000 MHz ("`C e`" command), your setting will be given by:

$F_{setting} = F_{desired}*938.249922368853/(F_{clk})$ MHz

where F_{clk} is your external clock in MHz.

NOTE:

You must account for your external clock frequency accuracy and calculation round-off when using an external clock. Most calculators have less than 48-bits of resolution.

The noise and accuracy specifications are directly affected by the quality of the external source. Unless care is exercised, your specifications may be degraded. Please verify your system requirements with the chosen clock mode.

4.10 For example, if you were using an OC-12 clock of 622.08 MHz, and desire a 10 MHz output, your calculation will be:

$F_{setting} = F_{desired}*938.249922368853/(F_{clk})$ MHz

$= 10.0*938.249922368853/622.08$

$= 15.08246402985$

Send: `F0 15.08246402985`

4.11 Since the internal frequency resolution of the 425A is 48-bits, the typical fractional frequency error (**Δf/f**) for output frequencies in the MHz range will be on the order of $1x10^{-12}$, even when exact values are not possible due the round-off from the external clock scaling. For the example, the 10.00 MHz error will be approximately 2 μHz when using an external 10 MHz clock, resulting in $2x10^{-13}$ **Δf/f**.

For many applications, this magnitude of the deviation will be insignificant.

NOTE:

The frequency command is limited to a maximum value of approximately 469.1 MHz, 50% of internal clock. The filter -3dB cut-off is set to 375 MHz. Distortion and roll-off will increase beyond 350 MHz, but the outputs may still be usable in your application.

4.12 The relative phase of the output is settable to 14-bits of resolution. The relative phase shifts by:

$$Phase_{out} = (P_{setting})*360^{o}/16384$$
$$P_{setting} = 0 \text{ to } 16383.$$

4.13 The amplitude of the sine output can be adjusted using the "`V0 N`" command. The 50 Ω terminated output amplitude as a function of the V0 setting is given by:

$$Amplitude = 0.5*[0.27+0.19*N/264]\ V_{rms}$$
$$\text{approximately } 0.14 \text{ to } 0.5\ V_{rms}.$$

4.14 The LVCMOS output has a divide-by-2 prescaler followed by programmable 16-bit divider, which allows the sinewave frequency to be divided by integers up to 131,072. Your application frequency may be created by various combinations of the F0, D0 and Pr commands. You should experiment to find the best performance range for your application.

4.15 For example, if you desired a clock signal of 1.00 kHz, you could obtain it by setting F0 to 10.00 MHz and using at D0 value of 9,999.

4.16 The duty cycle of the LVCMOS output is dependent upon the divide ratio. Odd divider values (even D0 command values) give output symmetry furthest from 50%. For example, a divide of 3 ("`DO 2`") will result in a 33% duty factor. Even values produce symmetrical duty cycle outputs. The prescaler setting does not affect the duty factor, since it is before the programmable divider.

4.17 When the LVCMOS output is enabled, the divider is set immediately upon the end of command. It is unaffected by the "`I`" command settings.

NOTE:

The relative phase of the LVCMOS output with respect to the Sine output is dependent upon frequency and divide ratio settings.

4.18 A Baud rate command is available if you wish to set a Baud rate different than the default value. The value set by this command is volatile and not saved in EEPROM to prevent loss of communication. Upon power up, reset or clear, the 425A reverts to 19.2 kBaud.

4.19 Kb command examples, with the value in hexadecimal:

```
Kb 78        ;9.6 kBaud
Kb 3c        ;19.2 kBaud
Kb 1e        ;38.4 kBaud
Kb 14        ;57.6 kBaud
Kb 0a        ;115.2 kBaud
```

4.20 Depending upon your system requirements, you may wish to enable non-standard Baud rates. The formula for the Kb setting is:

$$\text{Baud Rate} = 1152/N \text{ kBaud}$$

where N is the decimal value of the Kb command hexadecimal value. N=0 is not allowed.

NOTE:

You will need to verify non-standard baud rates in your system. Consult Novatech Instruments regarding permanent setting of 115.2 kB.

4.21 The "QUE" command returns a two-line hexadecimal string which represents the present instrument state. The default return values are:

```
02BA7DEF3000 0000 03FF 000000
2100 15
```

The meanings are:

`02BA7DEF3000`: binary 48-bit frequency (scaled by 3 from serial input value)

`0000`: binary phase (max: 3FFF)

`03FF`: binary amplitude setting (max: 03FF)

`000000`: binary divider value (max FFFF)

(Leading byte: 01=prescaler on)

`2100`: internal control registers

`15`: software revision as x.y, (1.5)

5.0 Theory of Operation

5.1 Please refer to the simplified System Block Diagram in Figure 2 for the following discussion.

5.2 At every cycle of the 425A master clock, the 48-bit Direct Digital Synthesizer (DDS) integrated circuit increments the phase of an internal accumulator by a value determined by the frequency setting loaded into the on-chip registers. This digital phase value is converted on-chip to a sinusoidal amplitude level and delivered to an on-chip 14-bit digital-to-analog converter. The analog signal from this converter is filtered by a 7th-order elliptical low pass reconstruction filter, amplified and sent to the SINE output connector.

5.3 The amplified Sine signal is diverted to a high-speed zero crossing detector to generate the LVDS output signal. The output of the detector is fed back into the DDS IC to supply the clock for the internal programmable divider.

5.4 The frequency generated by the DDS IC is determined by the binary 48-bit frequency word loaded into the frequency register on the 425A. The output frequency is given by:

$$F_{out} = F_{binary}*(100/3)*F_{clock}/2^{48} \text{ Hz}$$

Where: F_{clock} = 28,147,497.6710656 Hz (int.)
F_{binary} = Binary value in DDS IC.
(F_{binary} ranges from 0 to 2^{47}-1)

This reduces to:

$$F_{out} = F_{binary}*3.333\overline{3}\ \mu\text{Hz}$$

for the internal (default) clock settings. The binary setting is the customer's input setting scaled by a factor of three and converted to a binary value with the LSB having a weight of 10 μHz.

5.5 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the system clock frequency (F_{binary}<=2^{47}-1). While it is possible to generate an output near 50% of the clock, the distortion may be unacceptable. Therefore, the output is limited to approximately 40% (approximately 350 MHz) of the system clock and a 7th-order elliptical output filter is implemented on board.

6.0 PERFORMANCE TEST

6.1 Install the 425A as directed in Section 3. Connect your host controller and operate the 425A per Section 4. The test limits assume a stable environment of 18-28°C.

NOTE:

Allow the 425A to warm up for at least 15 minutes before performing any measurements. For best results, the 425A should be verified in an environment similar to its application.

6.2 See Table 2 for a list of recommended test equipment to perform the following measurements.

Table 2: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	500MHz, 50Ω	Tektronix TDS3052C
Frequency Counter	350MHz	HP53132A
Counter Time Base	10MHz, <±0.1ppm	Novatech Instruments Model 1450B
External Clock	250-1000 MHz	Customer supplied

6.3 **Verify Frequency Accuracy.** To verify the frequency of the 425A, set the output sequentially to each value in Table 3, with the clock source set to internal ("`C i`"). Connect the recommended frequency counter set to 50 Ω termination and 0.1 Hz resolution. Verify the limits show in Table 3. If you do not use an external frequency standard for the frequency counter, be sure to add the error of your

counter to the tolerance. (LSD = **L**east **S**ignificant **D**igit on counter).

Table 3: Frequency Test Points

Frequency	Tolerance
250 kHz	±0.375 Hz ±1 LSD
1 MHz	±1.5 Hz ±1 LSD
10 MHz	±15 Hz ±1 LSD
30 MHz	±45 Hz ±1 LSD
50 MHz	±75 Hz ±1 LSD
100 MHz	±150 Hz ±1 LSD
150 MHz	±225 Hz ±1 LSD
250 MHz	±375 Hz ±1 LSD
350 MHz	±525 Hz ±1 LSD

6.4 **Sine Out Amplitude Verification.** Set the frequency of the 425A to 10 MHz. Connect the 425A Sine Out to the oscilloscope set for 50 Ω termination. Set the oscilloscope to measure to RMS voltage using at least 16 averages. Verify a reading of 0.5 Vrms ±0.1 Vrms.

6.5 **Output Flatness Verification.** Verify that the outputs are flat with frequency by performing the following test: Connect the 425A Sine Out to the oscilloscope set for 50 Ω termination. Use the same setting up as the Sine Out Amplitude Verification. Note the 100 MHz voltage reading.

6.6 Set the 425A to the values of Table 3. Verify that the oscilloscope amplitude reading remains within ±3dB (a multiple of 1.414 to 0.707) of the value noted in the previous paragraph.

6.7 **External Clock Input Verification.** Connect a 10.0 MHz external clock source via a short coaxial cable to the **REF IN** BNC on the 425A rear panel. Issue the "`C r`" command. Set the frequency to 10 MHz without scaling. Verify that your reference signal meets the requirements in the specifications. Verify an output frequency reading of 10.0186525742 MHz. You will need to account for the accuracy of your 10.00 MHz source and your frequency counter.

6.8 If you are using a clock source of 250 MHz to 1000 MHz, you will have to calculate the proper scaling per Section 4.

6.9 This concludes the verification test of the 425A.

7.0 CALIBRATION

7.1 The 425A has two user adjustable components: Y2, frequency, and R37, output amplitude. Calibration should be performed only if the 425A fails the performance test or if the unit has been repaired. Routine adjustments are not recommended nor generally required. This procedure assumes that the 425A has failed the performance test or has been repaired.

WARNING:

Calibration should be performed only by qualified personnel. The on-board components are static sensitive.

7.2 The adjustments shown are set to 1/2 the specification values.

NOTE:

Allow the 425A to warm up for at least 15 minutes before performing any adjustments. For optimum performance the 425A should be calibrated in an environment similar to its installation.

7.3 **Frequency Adjust, Y2.** Set the output of the 425A to 10.000000 MHz. Connect your frequency counter with its input set for 50 Ω termination. Adjust Y2 using a non-metallic adjustment tool for 10.000000 MHz, ±7.5 Hz.

7.4 **Amplitude Adjust, R37.** Connect the Sine output to the oscilloscope set to measure RMS voltage, with a minimum of 16 averages. Set the oscilloscope for 50 Ω input termination. Leave the 425A output set to 10.00 MHz. Adjust R37 for 0.5 Vrms ±0.05 Vrms.

7.5 This completes the calibration of the Model 425A.

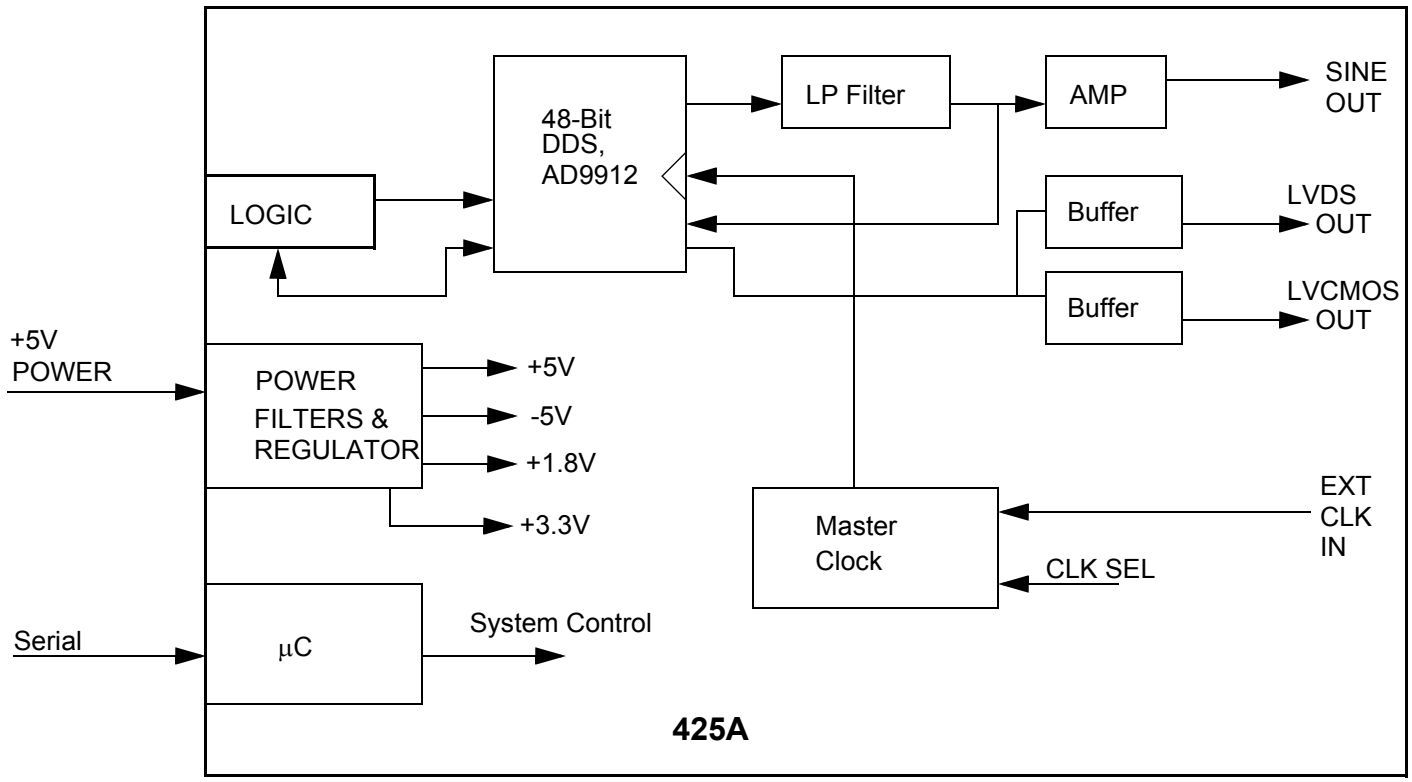

Figure 2.
Simplified System Block Diagram

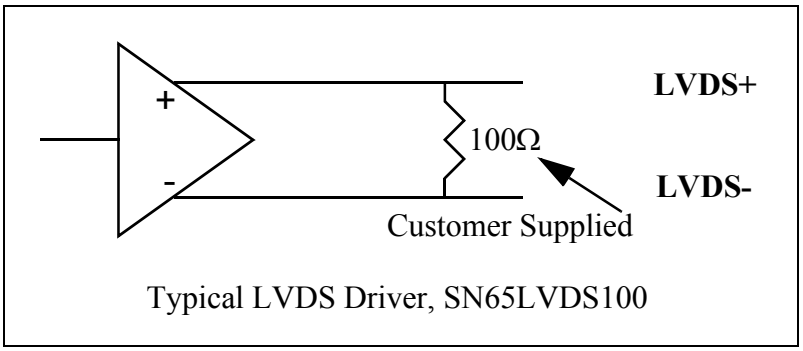

Figure 3.

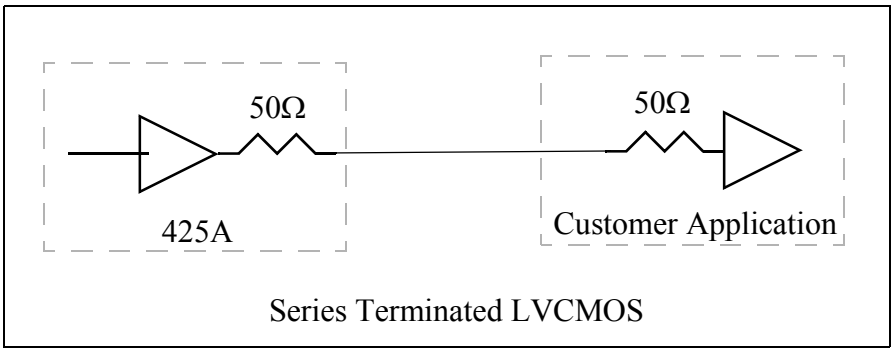

Figure 4.

425A MANUAL ERRATA

OPTION /E, Remote Clock

Option E makes it possible to use multiple 425A and have the outputs from these 425A be phase synchronous. Model 425A with Option E installed has the internal master 28MHz oscillator removed and two rear mounted SMA connectors installed. One of the rear mounted SMA connectors, labeled CLK IN, accepts a 28MHz clock signal from the 450A Clock Distribution Amplifier. The other rear mounted SMA connector labeled IOUD is intended to enable a future feature. When option E is installed on a 425A, the user needs to connect the 28MHz internal clock signal from a Model 450A Clock Distribution Amplifier to the 425A CLK IN SMA connector on the rear of the 425A and the 425A must be configured for internal clock (C x command where x=I, see table on page 4).

CAUTION: The 425A rear SMA connectors are intended for use with low voltage signals. Do not apply a voltage over 5.7Vpp AC on the CLK IN connector or you may damage the 425A.

WARRANTY

NOVATECH INSTRUMENTS warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS.

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